3D Process Simulation for Advanced Immersion Lithography

Shijie Wang, Ying Lin, Keng Heng Lai, Serene Tan, and Qun Ying Lin

***Abstract*—ArF immersion lithography has been widely adopted for advanced integrated circuits manufacturing since the 45nm technology node, and now is still one of the mainstream patterning techniques for semiconductor mass production. In this paper, we reported comprehensive evaluation results of a full track tri-layer coating immersion process for 28nm/20nm technology node applications, which included tri-layer process setup and film stack thickness optimization, illumination selection for establishment of printing 45nm line/space (L/S) and 65nm contact hole (CH) patterns. By combination of simulation and experimental verifications, a manufacturable immersion process has been successfully set up and optimized to meet customers' requirements.**

***Index Terms*—Immersion lithography, process setup, 3D process simulation, line/space, contact hole.**

I. Introduction

As a key patterning technique for modern integrated circuits manufacturing, ArF immersion lithography has been implemented since the 45nm technology node, and exploited to produce the 10nm logic node in 2017 and is highly expected to continue for the 7nm logic node and even further. [1, 2] The extensive and inclusive application of ArF immersion lithography with other resolution enhancement techniques (RETs) make it the most powerful, reliable and economical option from manufacturing perspective. [3] To suppress the impact of reflected light from underneath layers, the reflectivity must be precisely controlled at the interface of the resist and the bottom anti-reflective coating (BARC) layer. Dual BARC structure which contains an inorganic and an organic layer genuinely satisfied the requirements of both reflectivity control and pattern transfer during etch process. [4, 5] In particular, the all track processing tri-layer (resist/upper BARC/bottom BARC) stack has dominated the industry for years due to its simplicity and cost-efficiency. The upper BARC usually is a silicon containing anti-reflective coating (Si-ARC) layer and the bottom BARC normally is an organic spin-on carbon (SOC) layer. It is the application that determines the materials selection and thickness optimization. [5] In addition, when k_1-factor enters the ultra-low range (e.g., $k_{1=}$ 0.27- 0.30 for single exposure of 40- 45 nm half pitch by 1.3NA scanner), it poses big challenges for the best illumination condition design.

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In this paper, we focused on the technical aspects of establishment of a tri-layer immersion process, including from process setup to optimization through both theoretical simulation and experimental characterization. The goal was to build one manufacturable immersion process line capable of resolving 45nm line/space (L/S) and 65nm contact hole (CH) patterns with sufficient depth of focus (DOF) and exposure latitude (EL). It briefly included the determination of optimum thickness of Si-ARC and SOC layers, and the examination of appropriate illumination conditions for L/S and CH patterning which approached the tool limitations of single exposure.

II. Experimental

In this study, all the theoretical simulation was performed on PROLITH X5. The Si-ARC and SOC were selected in terms of their compatibility and topographical planarization performance as well as their n/k values for reflectivity control. To improve the predictive accuracy for resist exposure, we completed the resist model calibration and verification before its application on the process simulation. All the processes were established in our 12 inch manufacturing line with a 1.3NA scanner and automatic track system.

III. Results and Discussions

A. Tri-layer Thickness Determination

Fig. 1 showed a typical tri-layer film stack on a silicon substrate with silicon oxide (SiO) and silicon nitride (SiN) as two hard mask (HM) layers. Sometimes the top anti-reflective coating (TARC) layer is also accounted for one part of the tri-layer stack if a non topcoat-less resist is adopted, but the TARC thickness normally keeps constant. In a real scenario, the underneath SiO and/or SiN HM may be absent or replaced by other HM layer (e.g., TiN), or the sequence is reserved. In this study, we will demonstrate how to determine the optimum thickness of each layer to achieve the best reflectivity control under different scenarios.

Take 45nm L/S and 65nm CH patterning on Si substrate as two examples. Max NA=1.3, cross-pole and Quadropole illumination were applied, respectively. The n/k values for SOC, Si-ARC, resist and TARC at 193 nm are 1.45/0.25, 1.63/0.15, 1.66/0.04 and 1.525/0.002. As shown in Fig. 2 (a) and (b), the substrate reflectivity showed strong dependency on the Si-ARC thickness meanwhile the impact from the change of SOC thickness was trivial, which indicated the Si-ARC thickness played the key role for the overall substrate reflectivity control. It can be seen that when Si-ARC thickness

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is optimized, the substrate reflectivity keeps at minimum level with small variation even when SOC thickness changes broadly. The one set of optimum thickness, such as 34nm/200nm for Si-ARC and SOC, can make the substrate reflectivity at minimum level (<0.001) for both the Cross-pole illumination (Fig. 2(a)) and the Quadropole illumination (Fig. 2(b)). This implied that the one set of optimum Si-ARC and SOC thickness can be implemented for both L/S and CH patterning (refer to section *B* for more discussions). One advantage of sharing the same thickness for different patterning applications is that it can reduce the second set of thickness monitoring line in fab environment thus time and cost saving.

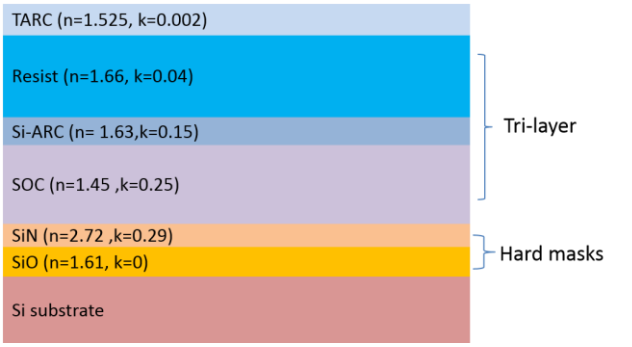

Fig. 1. A typical tri-layer stack on a silicon substrate with SiO and SiN hard masks.

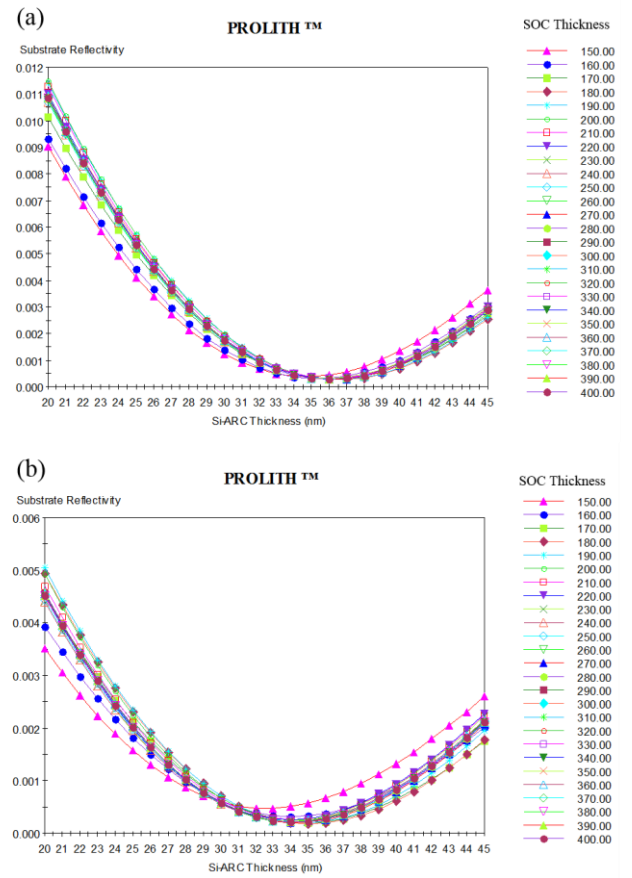

Fig. 2. The dependency of substrate reflectivity for the tri-layer stack on the thickness of SOC and Si-ARC. Using (a) cross-pole and (b) Quadropole illumination.

If the optimized Si-ARC and SOC thickness can fit all patterns from dense, to semi-dense and Iso structures is a big concern for immersion process when hyper NA applied. [6] Examination of the relationship among the incident light angle (Θ) on wafer, the thickness of Si-ARC/SOC and the substrate reflectivity can address this concern. In general, the large Θ is deemed normally from the diffracted light with small pith and vice versa. As shown in Fig. 3, to make the substrate reflectivity under an acceptable level (i.e., <0.01) for all pitch structures, it requires the SOC thickness being more than 100 nm. In this simulation, the optimum Si-ARC thickness was kept at 34nm as shown in Fig. 2.

Therefore, the tri-layer thickness determination for immersion process need consider more parameters than the single BARC process, especially when max NA was implemented.

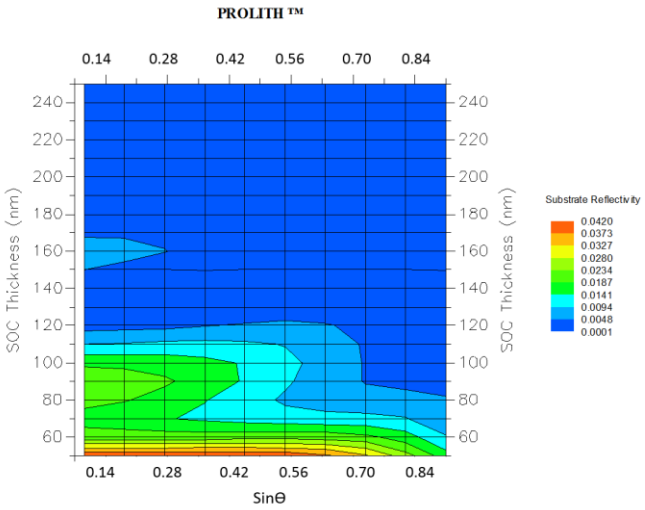

Fig. 3. The dependency of substrate reflectivity on the SOC thickness and the incident light angle.

B. Illumination Selection for Patterning 45 nm Dense Lines and 65nm CH

For the possible illumination for L/S pattering, we compared the DOF performance of Cross-pole, Annular and Conventional illumination modes, as shown in Fig 4(a). It is clear that the Cross-pole illumination showed the largest DOF for dense patterns in small pitch range. Not much DOF difference can be observed when patterns are in the semi-dense and Iso ranges. It is worthy to note that although the DOF performance was comparable for the three illumination modes, the resist profiles showed evident difference among them (profiles not shown). For instance, much more resist loss has been observed for conventional mode to resolve the 45nm lines (45nm line/110nm pitch) than those from using Cross-pole illumination. The resist loss difference can be as high as 76% for the two illumination modes during our simulation. Therefore, resist loss behavior is also one of the important parameters which need our attention when scrutinizing the best illumination candidates.

For the 65nm CH patterning, the DOF performance among Quadropole, Annular and Conventional illumination modes showed remarkable difference at the dense/semi-dense range, as shown in Fig. 4(b). The DOF for Quadropole at 130nm pitch is double of the DOF from Annular/Conventional illumination. This extraordinary ability to exposure dense CH

with sufficient DOF made Quadropole illumination as the best choice for 65nm CH patterning. The reason why we care so much of the performance in the small pitch range is that the printability can be much improved by optical proximity correction (OPC) for semi-dense/iso patterns with large pitches, such as through adding sub-resolution assisting bar (SRAF). However, there is no much room for SRAF and/or patterning sizing up for dense patterns.

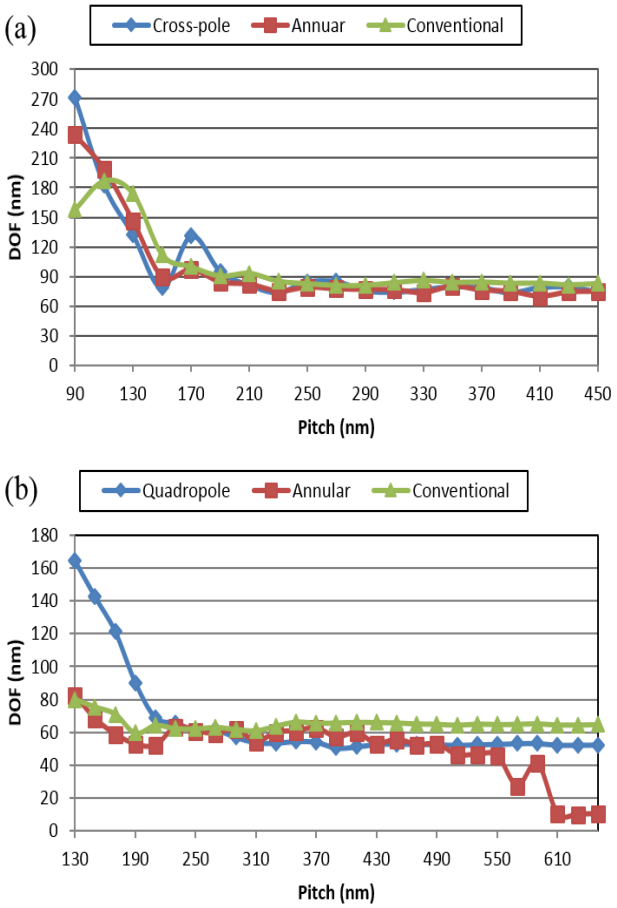

Fig. 4. The DOF performance of different illumination conditions to expose (a) 45nm line and (b) 65nm CH.

C. Mask Bias Determination for CH

When using phase-shifting mask (PSM) to expose CH patterns, one of the concerns is the printability of side-lobes due to the light that is transmitted through the chrome areas. To solve this issue, mask bias is often used as a simple OPC to eliminate this effect and enlarge the process window [7, 8]. As a starting point, we completed the simulation of applying mask CD bias from 0 to +50 nm to check how it affects the process window and side-lobes of 65nm CH/130nm pitch dense patterns. It was noted that the mask bias had trivial impact on the DOF, the delta (DOF_{max}- DOF_{min}) is less than 20nm (data not shown). The best DOF (164 nm) was achieved when mask bias was +30 nm. Fig. 5 showed the simulated resist profiles for the +30 nm bias CH patterns exposed by the Quadropole illumination. No side-lobes was observed in Fig. 5(a) and it kept the same even when focus shifted from the best conditions (profiles not shown).

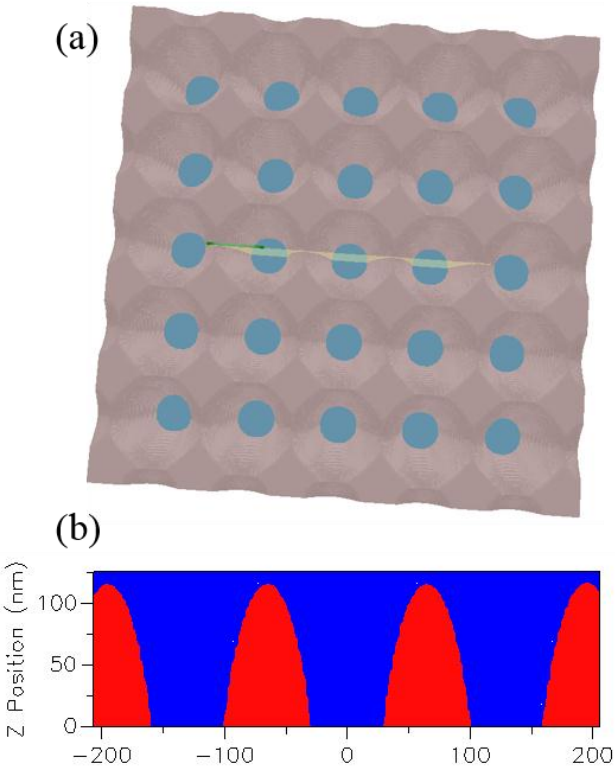

Fig. 5 (a) and (b) are the simulated 3D and cross-sectional resist profiles for the 65nm CH/130nm pitch dense patterns with a +30 nm CD mask bias.

D. Experimental Verification

From the above simulation, the best illumination for 45nm L/S and 65nm CH patterning are Cross-pole and Quadropole illumination, respectively. The best mask bias for 65nm CH/130nm pitch is +30nm. To verify our simulation's accuracy, the experiments were carried out in a fab environment. The exposure conditions were summarized in Table I.

TABLE I: ILLUMINATION CONDITIONS FOR EXPERIMENTAL VERIFICATION

Task	Illumination Conditions
LS Patterning (L/Pitch: 45nm/90nm)	1.3NA, Cross-pole: sigma center=0.882, sigma radius=0.092 Azimuthal polarization
CH Patterning (CH/Pitch: 65nm/130nm)	1.3NA, Quadropole: sigma center=0.792, sigma radius=0.088 W/o polarization +30nm CD bias

Fig. 6 (a) and (b) displayed the experimental focus exposure matrix (FEM) results of 45nm L/S and 65nm CH/130nm dense patterning using the tri-layer immersion process developed in the previous sections. Both L/S and CH patterns were fully resolved without pattern collapse and side-lobes. The EL and DOF margins were big enough from manufacturing perspective. It proved the methodologies adopted for the immersion process setup were right. To make patterns are printable with sufficient process margins in a full pitch range, more work need to be done with the help of OPC. The relevant work is in progress.

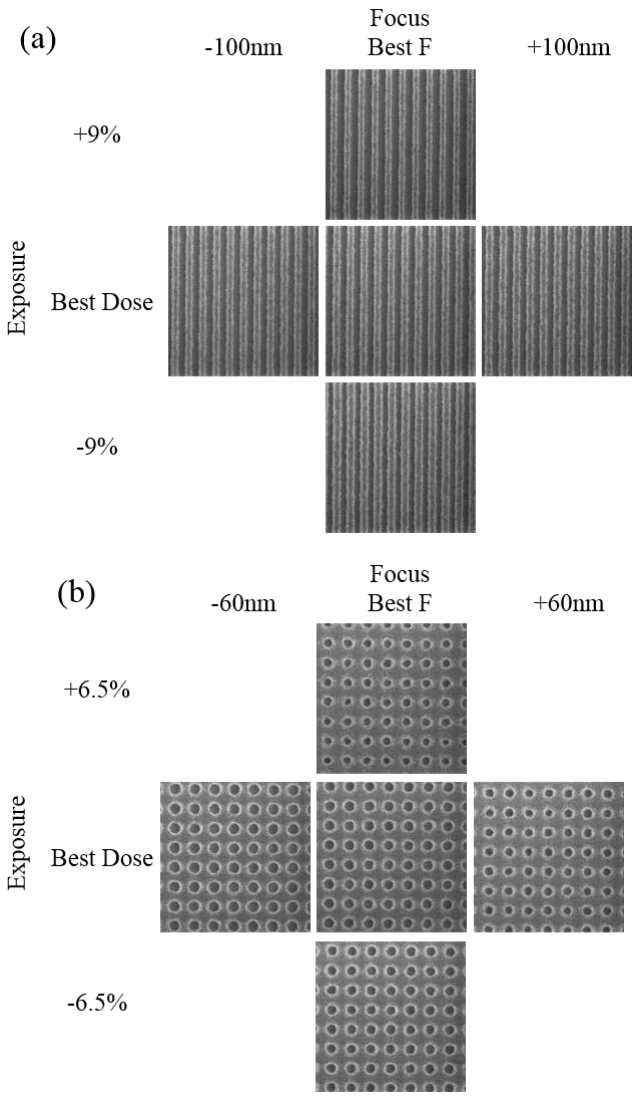

Fig. 6. The experimental focus exposure matrix (FEM) results of 45nm L/S and 65nm CH/130nm dense patterns developed by a tri-layer immersion process (1.3NA).

IV. Conclusion

In this paper, we reported comprehensive evaluation results of a full track tri-layer coating immersion process for 28nm/20nm technology node applications from both theoretical and experimental perspective. From simulation, it was found that Si-ARC thickness played the dominant role in determination of the substrate reflectivity level. In contrast, the impact from SOC thickness was minor once its thickness was higher than one value (such as > 100nm in our case). Cross-pole and Quadropole illumination modes were found to be the best illumination types for exposure of 45nm L/S and 65nm CH dense patterns in terms of DOF and resist profiles. Process window evaluation on physical wafers showed sufficient process margins (EL and DOF) for both LS and CH patterning. By combination of simulation and experimental verifications, a manufacturable immersion process has been successfully set up and optimized to meet customers' requirements.

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