A Real Measurement Power Tool for Intellectual Property on FPGA

N. Chalbi, M. Boubaker, and M. H. Bedoui

***Abstract*—The FPGA (Field Programmable Gate Array) power consumption has become a very critical problem for new technologies. Also, in order to develop embedded systems it is necessary to controll this parameter at a high level of the conception design. For these reasons, we present in this paper an RTL (Register Transfer Level) IPs (Intellectual Property) power models. The characterization phase of the dynamic power variation was carried out by using a real power measurement tool organized around of the XC2VP4 (Virtex-II Pro) device. The RTL models were elaborated according to the clock frequency and input activity rate. The accuracy of the adopted methodology has been justified by comparing our results with the UAM (University Autonoma Madrid) and the Xilinx Xpower tools.**

***Index Terms*—FPGA power consumption, real power measurement tool, characterization, accuracy.**

I. Introduction

The digital integrated circuits have invaded all the fields such as communication and car industries. The FPGA as a reprogrammable circuit has become the most adopted support thanks to its flexibility and its fast prototyping. The latter presents an important implementation surface and a higher clock frequency caused by the CMOS (Complement MOS) technology advances and the increasing development of CAD tools. Despite these advantages, the FPGA supports present a problem related to the power consumption which depends on several parameters. Moreover, the development technology has generated an increase in the number of on-chip systems. These embedded systems require a very low operation power. Therefore, it is very significant to evaluate this factor. In the current technology, the consumption power has become a criterion of high level design. The success of these FPGA designs makes the suppliers firstly explore the whole environment in order to provide an accurate power characterization methodology and secondly seek a suitable optimization.

The consumption evaluation is the most difficult problem since it depends not only on the FPGA circuit but also on the implemented application. The number of tools suited to estimate the power is limited. We can mention the Xpower tool [1] provided by Xilinx company and the Powerplay tool [2] from Altera. These commercial tools are based on a capacitive model and estimate the power after the placement/routage phase. The different estimation power methodologies have been applied at the various conception levels: low-level or high level (system, algorithmic and architectural). Several works in the literature have addressed this problem, and a comprehensive survey was presented in [3]. The low-level techniques can be classified into simulation and stochastic methods. In the simulation methodologies [4]-[6], some test vectors were used to simulate the design and estimate the switching probabilities followed by a distributed power analysis. The advantages of these techniques are that the simulators at are available this level and the correlations between the inputs are taken into account. As a result, the interconnections consume 52% of the total power, the logic 26% and the clock 22%.

Other methods were based on measuring the currents by adopting the incremental approach [7]. The tests were carried out on the Xilinx XC400E device and Altera Flex10K100 and showed that most power is consumed by the CLB (Lut+DFF) and the interconnections while the clock consumes only 10% of the total power. For the methods based on stochastic techniques [8]-[10], the authors used the entropy concept to approximate the activity rate. These techniques allow fast runtime and weak dependence between the inputs.

The high level methodologies can be categorized in macro-models techniques and the FLPA (Functional Level Power Analysis) method. The latter which was presented in [11],[12] consists of three phases. The first is dedicated to the functional analysis by enumerating the different algorithmic, architectural and technological parameters influencing the power. The second phase is called power characterization according to these parameters. The last one allows the extraction of the mathematical model. In the macro-model category, various models were developed. In [13], the probability concept was proposed for the first time by using a zero-delay model while considering a spatial and temporal independence between the inputs. In [14], the authors presented a new approach based on the probability and spatial correlation parameters. This latter adopted the spatial dependence hypothesis among the signals, hence the effect of high runtime and good accuracy. This model was extended to a probabilistic-simulation one which treated the temporal dependence [15]-[18]. In [19], the author proposed a power macro-model at the RTL (Register Transfer Level) level. The IP (Intellectual Property) input sequences were generated by a genetic algorithm followed by a zero Monte-Carlo simulation.

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The works in [20]-[24] developed some macro-model powers while exploiting the low-level design characteristics. These models were based on certain statistical parameters such as probability, transition density, spatial and temporal correlations.

The accuracy of different models depends on the CAD tools accuracy, the approximation taken to carry out the models and also on the estimation design level. We propose in this paper a real power estimation methodology based on the FPGA Virtex-II Pro board. The results of this method will be exploited on an RTL level power estimation tool.

The paper is organized as follows. Section 2 presents the FPGA environment. The description of our measurement methodology is done in section 3. The implementation and the dynamic power measurements of certain IP cores are explained in section 4. We reveal the results and the validation of our approach in section 5. Finally, the conclusion and future work are given in section 6.

II. The VirtexII- Pro Environment

A. Description of the FPGA Internal Architecture

The FPGA architecture consists of a matrix of configurable logic blocks (CLB), configurable I/O blocks, and programmable interconnections. Also, there is a clock circuitry for driving the clock signals to each logic block. The latest generations also include the DLL (Digital Locked Loop) blocks, the memory RAMs blocks, the multiplier blocks and the processor cores. The leading-edge 0.13µm CMOS nine-layer copper process and Virtex-II Pro architecture are optimized for high performance designs in a wide range of densities. Combining a wide variety of flexible features and IP cores, the Virtex-II Pro family enhances programmable logic design capabilities and is a powerful alternative to mask-programmed Gate arrays [25].

Fig.1 illustrates the generic architecture of the xc2vp4 device, while tableI summarizes the whole target resources [25].

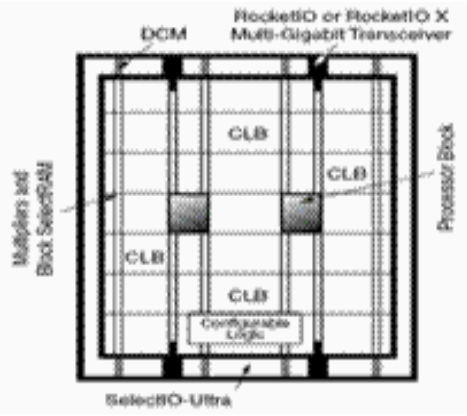

Fig. 1. Virtex-II Pro Generic Architecture

TABLE I: XC2VP4 Ressources

CLB	18*18 Bit Multipliers blocks	Blocks Select Rams (18 kb blocks)	I/O	DCM
3.008	28	28	348	4

B. Power Consumption in SRAM-Based FPGA

The power consumed by any CMOS device can be divided into two components [26]:

- The static portion is caused by the current leakage through the device. The static current is based on the device temperature, process and voltage parameters. It is highly dependent on temperature, which has a circular dependence upon the thermal characteristics of the device-board combination. The static power is the leakage through all the power supplies.
- The dynamic portion of power consumption is the power consumed by the used resources while they are switching. The dynamic portion's power dissipation is proportional to the frequency at which the resource is running as well as the number of resource units used. This dynamic portion has two components:
  1) Short-circuit which is due to the DC path between the supply rails during output transitions.
  2) Switching which is dissipated when capacitive loads are charged and discharged during logic changes.

III. FPGA Power Estimation Methodology

In this part, we describe our methodology to estimate FPGA consumption. We have developed an experimental bench organized around the XC2VP4 device (package ff672). The dynamic power has been modeled according to the clock frequency and the activity rate (Fig.2.). The obtained models have been compared with other works elaborated in [27]-[30] for the same application.

A. Description of the Measurement Procedure

Our methodology consists in measuring the currents and voltage consumed by the internal logic and the input/output FPGA application. To carry out this, we placed two true RMS ammeters on the output of the voltage regulators 1.5 V and 2.5 V (Fig. 2), while using the jumpers accessible on the FPGA board [25].

The adopted environment enables us to measure:

- The static power (P_s) which is consumed by the FPGA before the application configuration or when neither stimulus nor clocking is applied.

$$P_S = I_1 V_1 + I_2 V_2 \quad (1)$$

Where: I_1 is the current consumed by the FPGA core, I_2 is the current consumed by the input/output pins; V_1: FPGA core voltage; V_2: input/output voltage.

- The total power of the application under test (X Application with the input vector generator).

$$P_{total} = P_{static} + P_{dynamic} \quad total \quad (2)$$

The total power of the generator circuit whose dynamic power is deduced according to the following formula:

$$P_{dyn} = P_{total} - P_{static} \quad (3)$$

- The dynamic power can be measured by varying the clock frequency and the activity rate. The circuit activity is obtained by switching the input vectors. For that purpose and to avoid the use of external signals, we have decided to add a sequence generator to the circuit under test. This circuit is architectured around an FSM (Finite state Machine) and is controlled by the reset signal (if reset='1' no input generated and if reset='0' generation of sequences.). An activity rate has a value of 100% when each bit changes state after each clock cycle. So we can define the input switching frequency in Mhz by this equation for a desired activity rate Fa (%):

$$F(Mhz) = \frac{1}{2} \times F_{clk} \times Fa(\%) \quad (4)$$

- The I/O consumption by configuring applications with I/O and zero internal logic (Table III).

A detailed description of our methodology is illustrated in fig.2 below.

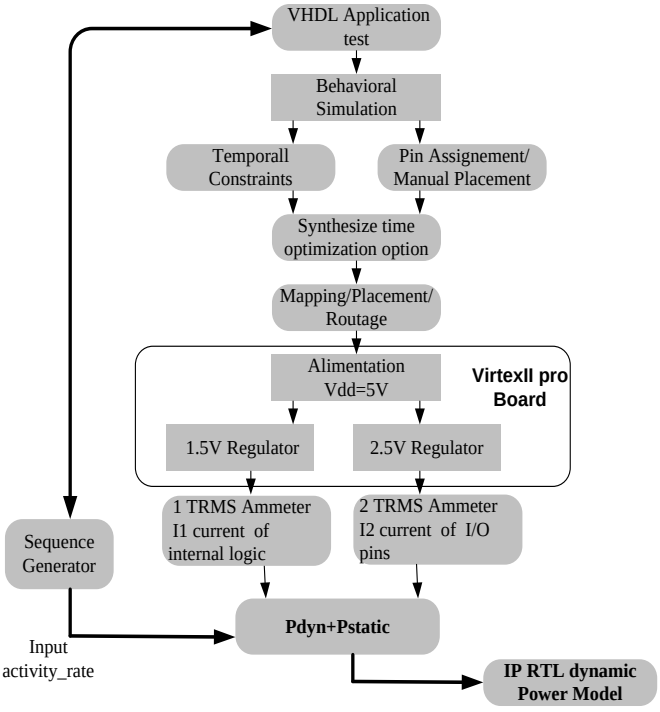

Fig. 2. Power characterization methodology

B. Description of the UAM Tool

The experimental methods developed to characterize power are very limited. We have chosen to compare our measurement results with those from the UAM (University Autonoma Madrid). This environment is described in (Fig. 3):

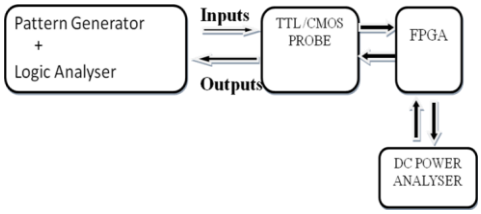

Fig. 3. Power measurement tool architecture

IV. Implementation and Measurement

By adopting this methodology, we have succeeded in establishing in the first phase an accurate measurement power of certain arithmetic IPs (based on adders and multipliers). In the second phase, we have elaborated some RTL models for the dynamic power variation by applying a linear interpolation. The entire application test is described with the VHDL (Very High Speed Integrated Hardware Description Language) language, using the Xilinx ISE (Integrated Software Environment) environment.

A. Sequence Generator Performance

The surface in terms of CLB numbers and the power consumption of the various generators are summarized in the following table. The results have been obtained for a fixed frequency (F=100 MHz) and varied input activities (a minimum activity had a value as 19%, an average activity have been fixed to 50% and a maximum activity have been fixed at 95%).

TABLE II : Input Sequence Generator Performances

Bit Width	*CLB Number*	P dyn(mw/MHz)		
		min_ activity	avg_activity	max_activity
4	6	0.095	0.204	0.273
6	16	0.157	0.269	0.370
8	32	0.256	0.368	0.450
16	61	0.403	0.656	0.807
32	120	0.756	1.207	1.563

B. RTL Models of Arithmetic Components

The dynamic power variation of an 8 bit adder and an (8×8) bit multiplier, according to the clock frequency, are described in fig.4. These variations can be approximated by linear functions for an average activity as follows:

- For an 8 bit adder:

$$P_{dyn}(F) = 32.174 \times F - 35.454 \quad (5)$$

- For an (8×8) bit multiplier:

$$P_{dyn}(F) = 106.93 \times F - 112.06 \quad (6)$$

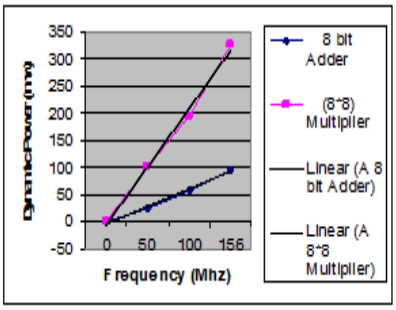

Fig. 4. Dynamic Power of an 8 bit Adder and an (8*8) Multiplier versus frequency

We have also implemented multiplier circuits with various input bit widths (4, 6, 8). Figure 5 shows that the activity rate affects more the dynamic power than the frequency factor. It outlines the linear dependence between dynamic power and activity rate for a fixed frequency of 100 MHz.

- For a (4×4) multiplier :

$$P_{dyn}(activity\_factor, F) = [0.717 \times activity\_rate - 0.2793] \times F \quad (7)$$

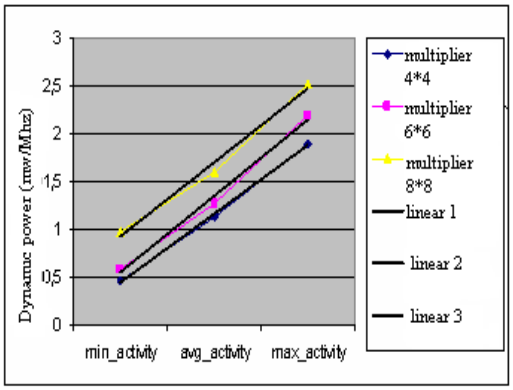

Fig. 5. Dynamic power of multipliers versus activity factors

- For a (6×6) multiplier :

$$P_{dyn}(activity\_factor, F) = [0.798 \times activity\_rate - 0.2543] \times F \quad (8)$$

- For an (8×8) multiplier:

$$P_{dyn}(activity\_factor, F) = [0.768 \times activity\_rate + 0.1559] \times F \quad (9)$$

C. I/O Dynamic Power Measurement

By using our tool, it was possible to determine the input/output power consumption by configuring on FPGA only I /O applications. The first column of table III describes the number of I/O used. The second column illustrates its corresponding utilization rate and the last one illustrates the consumed dynamic power in mw/Mhz.

TABLE III: DYNAMIC POWER (MW/MHZ) VERSUS I/O UTILIZATION RATE

IOBs	Utilization rate (%)	P dyn(mw/MHz)
35	10	2.279
70	20	2.404
140	40	2.405
209	60	2.455
280	80	4.258
348	100	5.081

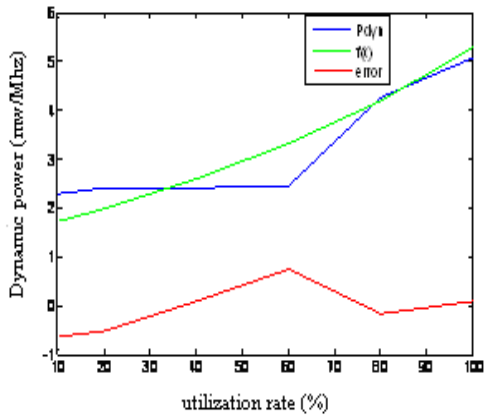

Fig. 5. Dynamic power versus input/output utilization rate and its f(x) approximation function

The I/O dynamic power variation (curve in blue) has been approximated to the exponential function (curve in green) by matlab interpolation. The error function between the two variations is described by the curve in red:

$$P_{dyn}(N_{I/O}, F) = \left[(2.2 \times exp^{(0.01 \times x)}) - 0.7 \right] * F \quad (10)$$

$$x = \frac{N_{I/O}}{N_{I/O\ total}} \text{ is the } I/O utilization\ rate(\%)$$

V. RESULTS AND VALIDATION

At first, we measured the consumption of the same applications (adders and multipliers) by using the two tools . Figure 7 illustrates a comparison between every methodology and shows the accuracy of our method. The blue histogram describes the dynamic power consumed by the multipliers (multiplier1, adder1: dynamic power using our methodology) and (multipliers2, adder2: dynamic power using the UAM tool [30] for a minimum activity. The red histogram describes the same dynamic power for an average activity where as the third one outlines this variation for a maximum activity. This figure shows that the variation between the two methods is 4.8%, which justifies the accuracy for our tool .

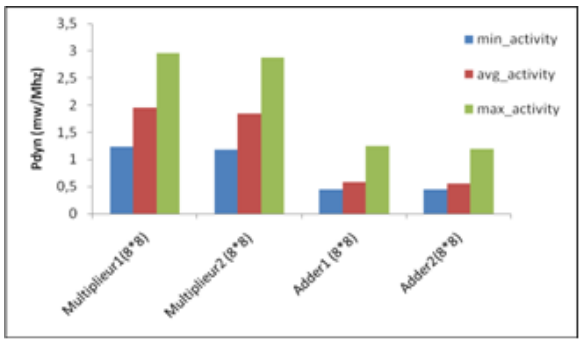

Fig. 6. Dynamic Power of a multiplier (8*8) bit and an adder 8 bit function to the activity rate by using the two tools

Then, we compared the results from the two methodologies with the estimated model (Table IV). The first column describes some arithmetic test applications, the

second column shows the dynamic power measured by the UAM tool, the third column illustrates our measuring tool results, the fourth column presents the estimated dynamic power by adopting the IP mathematical models, and the last two columns show the variation between the three methods.

The resources occupied in terms of surface (Slices, Luts, IOBs) and dynamic power obtained by our measurement tool (for a frequency F=100 MHz and an average activity rate) and the Xpower tool are displayed in tableV. As test applications, we have chosen an FIR filter (8 bit input and 32 coefficients, every coefficient has an 8-bit precision). Its RTL architecture includes 26 (8×8) bit multipliers, 31 adders/substractors, 250 registers and 62 XOR gates. The second application is a sequential divider algorithm of two 4-bit signed numbers, and it is formed by 4 substractors and 4 comparators. The last one is the exponential function which consists of a ROM (Read Only Memory) component, two 8-bit input comparators and a linear function ($a \times x + b$).

TABLE IV: COMPARISON BETWEEN THE TWO MEASUREMENT POWER METHODOLOGIES AND THE ESTIMATED ONE

Application	Pdyn1 (mw/Mhz)	Pdyn2 (mw/Mhz)	Pdyn.es (mw/Mhz)	Pdyn. es -Pdyn2	Pdyn.es - Pdyn1
multipler+ adder in series	1.787	1.943	1.3762	-0.56	-0.41
5 parallel (8×8) Multipliers	6.97	7.238	5.290	-1.948	-1.68
10 parallel (8×8) Multiplier s	11.537	13.002	10.58	-2.42	-0.95
15 parallel (8×8) Multipliers	16.84	18.25	15.87	-2.38	-0.97

TABLE V: COMPARISON BETWEEN OUR TOOL AND XILINX XPOWER

Application	Slices	Pdyn (mw/Mhz)	Pdyn.Xpower (mw/Mhz)	ΔP
FIR	733	1.418	1.71	0.29
Divider	35	1.66	1.91	0.25
$\sum_{i=1}^{23}(X_i - W_{ij})^2$	772	2.495	2.99	0.50
4 input (8bit) comparator	46	0.014	0.02	0.005
ROM (23 words×8 bit)	4	0.049	0.07	0.02
RAM(23 words×8 bit)	16	0.339	0.41	0.07
Exponential function	62	0.071	0.09	0.024

VI. CONCLUSION

This paper has presented an experimental power measurement methodology. It describes a simple and accurate method using the current measurement. The characterization results were exploited to establish some RTL models. For the activity variation, we have used inputs sequences generators which are included with the application under test instead of adopting another FPGA device to send these sequences. We are currently exploring several architectures that might fit the RTL models more adequately.

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