A Piece Wise Linear Memristor Model with Switches

Ahmet Solak and Saadetdin Herdem

***Abstract*—Memristor is firstly published by L.Chua in 1971. It is derived from relationship between charge and flux. Thus, memristor take its place as fourth passive circuit element with resistor, inductor and capacitor. After it is physically realization in 2008 by S. Williams and his teammates, interest in memristor and studies about it quite increase. PWL (PieceWise Linear) memristor model is one of the memristor modeling style. This model proposes a new equivalent memristor model by linearizing I-V characteristic of memristor. Linearization process may vary from study to study. In this paper, we suggest a new PWL memristor model and its equivalent analog circuit. The proposed model in this paper is independent from frequency. The results obtained by using this model are sufficiently compatible.**

***Index Terms*—Control equations, equivalent circuit, memristor, PWL model.**

I. Introduction

Memristor is short form of memory resistor. It is firstly proposed by nonlinear circuit theorist Leon Chua in 1971 [1]. He described a new passive circuit element which is derived from relationship between electric charge and magnetic flux "M=dϕ/dq". Fig. 1 shows relationship among passive circuit elements. Thus, the missing link among charge, flux, voltage and current is completed. So, memristor took its place as fourth passive circuit element with resistor, capacitor and inductor. It has a memristance whose symbol is "M" and characteristic of memristance similar to resistance.

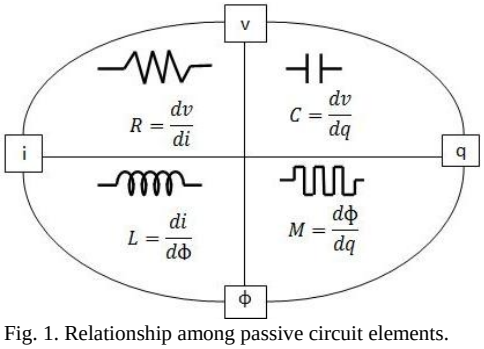

Fig. 1. Relationship among passive circuit elements.

In 2008, Stanley Williams and his team from HP (Hewlett-Packard) Research Laboratories published a new paper which includes first realized memristor as a physical device [2]. This memristor model is in nanoscale size and consists of doped and undoped TiO_2 between two thin Pt layers. Undoped TiO_2 part has pure TiO_2 and its resistance is higher than other part.

Doped TiO_2 part is doped with oxygen vacancies which make it conductive and lower resistance. When electric charge flows from undoped side to doped side, the resistance of memristor decreases. In reverse situation the resistance of memristor increases.

Fig. 2 shows HP memristor model. In this figure, w represents Doped TiO_2 part and D represents whole TiO_2 part. There is a thin film between these parts and with the flow of electric charge memristance of memristor model change due to the fact that position of thin film change between parts.

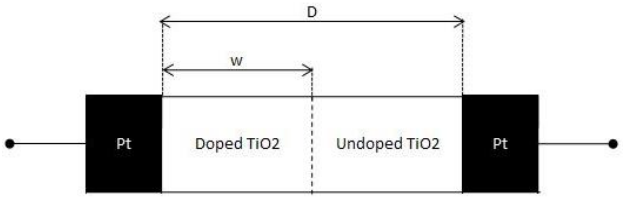

Fig. 2. Memristor model adapt from [2].

According to this model, R_{ON} represents doped TiO_2 part and R_{OFF} represents undoped TiO_2 part. R_{ON} and R_{OFF} represent limit values of memristance. R_{MEM} represents memristance value and changes depending on R_{ON}, R_{OFF} and w/D ratio. w/D ratio represent proportion of doped and undoped parts proportion which is shown in (1). From this equation x is found and when put this value to (2), R_{MEM} value found.

$$x = \frac{w}{D} \tag{1}$$

$$R_{MEM}(x) = R_{ON}x + R_{OFF}(1-x) \tag{2}$$

After this paper was published, HP announced that physical memristor device would be brought to market within a couple of years but it is not produced yet. So, memristor models, memristor equivalent circuits and memristor emulator circuits become more important for memristor research and memristor based applications.

With this study, interest in memristor is quite increase and also motivate the study of new design paradigms and applications. New memristor models, emulator circuits, applications like programmable logic, signal processing, neural networks, control systems, brain –computer interfaces and etc. are became new study fields about memristor [3]-[10].

In this study, high resistance R_{OFF} and low resistance R_{ON} are obtained from chemical properties of elements between pure TiO_2 and doped TiO_2 with oxygen vacancies respectively. So you should know also chemical properties of

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elements for analyzing this study. On contrary to this memristor model, PWL memristor model is only derived from I-V characteristic of memristor and so it is simpler than other memristor model and more feasibility. Goal of PWL memristor model is that achieve a new memristor model by ignoring chemical properties of elements. Many PWL memristor model published since memristor became popular [11]-[14].

In this paper, we propose a new PWL (Piecewise Linear) memristor model. And we view our study under methodology, results and conclusion titles. In methodology part, we mention about PWL theory and our model; in results part we mention about our models results and comparison among our results and other published papers and in conclusion part we mention about conclusions of study respectively.

II. Methodology

In this part, we view memristor model in two subtitles. These are theory and circuit model. In theory part, we define PWL memristor model and also analyze our new PWL model. In circuit model part according to giving memristor model we get an equivalent memristor model.

A. Theory

In theory, memristor has a hysteresis I-V characteristic is shown in Fig. 3 (a). It is hard to analyze this graph because of its hysteresis curve. So PWL memristor model is derived as a model of memristor which obtained by linearization of I-V characteristic of memristor shown in Fig. 3 (b) [14].

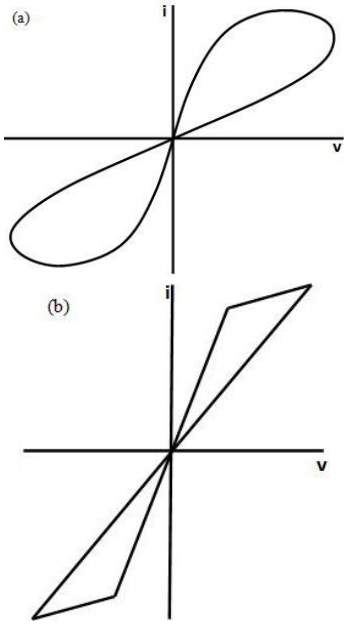

Fig. 3. (a). I-V characteristic of memristor (b). I-V characteristic of PWL memristor model [14].

Similar to this study we propose a new I-V characteristic of memristor and also a new PWL memristor model. Fig.4 shows I-V characteristic of proposed memristor model. While we design this model, take into account I-V characteristic design parameters from [15].

B. Circuit Model

When we examine I-V characteristic of memristor is shown in Fig.4, it can be divided into four regions. Voltage and current parameters approximately selected as follows: V1=1.888 V, V2=3.999 V, I1=1.525 mA, I2=0.5625 mA. These regions are determined by using control equations as shown in Table I.

According to Table I, we start modeling equivalent memristor circuit model. In first region, the characteristic is similar to I-V characteristic of a resistance and so we can use a resistance for this region in circuit. In second region, the characteristic is similar to characteristic of a negative resistance and a positive DC voltage source. In third region, the characteristic is similar to characteristic of a resistance too like first region; but voltage-current proportion is more less than first region so it has a smaller resistance value than first region. In fourth region, the characteristic similar to the characteristic of second region; but the difference between two regions is that in second region DC voltage source is positive; but in fourth region it is negative.

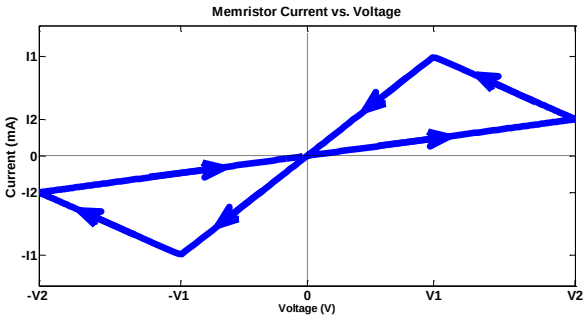

Fig. 4. I-V characteristic of proposed memristor model [15].

TABLE I: The Arrangement of Regions

Regions	Voltage	$\frac{dv}{dt}$
1.Region	[-V2,V2]	$\frac{dv}{dt}>0$
2.Region	[V1,V2]	$\frac{dv}{dt}<0$
3.Region	[-V1,V1]	$\frac{dv}{dt}<0$
4.Region	[-V2,-V1]	$\frac{dv}{dt}<0$

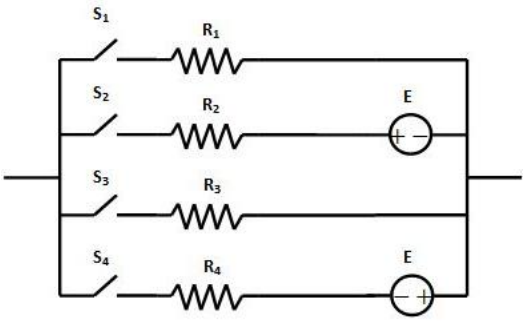

Fig. 5. Proposed memristor equivalent circuit.

With this I-V characteristic analysis, a new memristor equivalent circuit is proposed as shown Fig. 5. This circuit could be applicable so simple because it is clearly seen that it

consist of only resistances and DC voltage supplies. According to calculations from analysis, resistance and DC voltage values should be selected as follows: R1=7.1093 kΩ, R2=R4=-2.1932 kΩ, R3=1.2380 kΩ, E=5.2322 V.

In this circuit, switches present each region respectively. At initial state, S_1 is closed and other switches are opened. For a period (T=1 ms), obtained closed times of switches by using control equations shown in Fig.6. From this figure, closed times of switches written more detailed shown at Table II. In here, there are small time differences between two switches transition. It can be called as transition time and it is about 0.002 - 0.003 ms so it can be underestimated.

TABLE II: CLOSED TIMES OF SWITCHES

Switches	Times
S_1	[0, 0.245 ms] & [0.75 ms, 1 ms]
S_2	[0.25 ms, 0.415 ms]
S_3	[0.417 ms, 0.582 ms]
S_4	[0.585 ms, 0.747 ms]

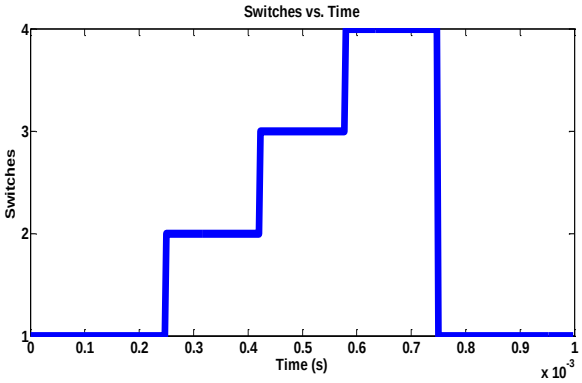

Fig. 6. Switch States for a period (T=1 ms).

III. RESULTS

In this part, we verify our proposed model by comparing with published paper given at references [15], [16]. When we examine our I-V is shown in Fig.4, it is similar to I-V characteristic of Vourkas & Sirakoulis model [15] and also Joglekar & Wolf memristor model [15], [16]. Fig. 7 shows comparison among three I-V characteristics. In this figure, blue graph represents our memristor model, red graph represents Vourkas & Sirakoulis model [15] and green graph represents Joglekar & Wolf memristor model [15], [16].

As shown in Fig. 7 I-V characteristic of our proposed memristor model and other characteristics are almost same. There are little differences among our graph and other graphs. And the differences among our graph and others is because of that our model is linear so it has a linear I-V characteristic; but others have hysteresis I-V characteristic because of memristor original I-V characteristic. Except that there are no big differences among characteristics.

Fig. 8 shows comparison among M-V characteristic of three memristor models. In this figure, blue graph represents M-V characteristic of our proposed model, red graph represents M-V characteristic of Vourkas & Sirakoulis memristor model [15], green graph represents M-V characteristic of Joglekar & Wolf memristor model [15], [16].

When these characteristics compared, it is seen that they are similar to each other with the outline; but at some points vary our M-V characteristic. The reason is that our model is linearized memristor model was mentioned about comparison of I-V characteristics part. Other models as shown in Fig. 7 have hysteresis I-V characteristic so have curved M-V characteristic. Also, because of first and last voltage and current values are 0(zero) memristance values go to infinite. So a gap occurs at these points in our M-V characteristic.

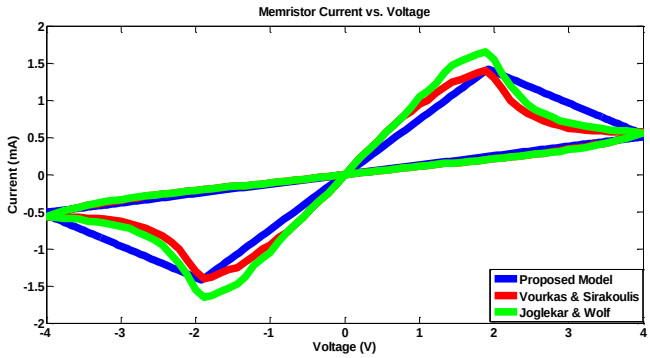

Fig. 7. Comparison among I-V characteristic of memristor models.

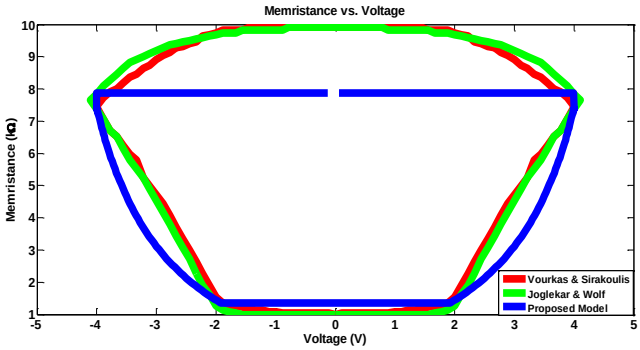

Fig. 8. Comparison among M-V characteristic of memristor models.

All in all, our proposed memristor model is compared with two published and verified memristor models. Not only I-V graph of memristor but also M-V graph of it provides this memristor models except small differences. And this differences stem from our model linearity as mentioned before. Besides, realization of circuit model is so simple because it has four resistances, four switches and two DC voltage supplies as shown in Fig. 5. And also switching time among switches is sufficient and consistent as shown in Fig.6 and at Table II.

IV. CONCLUSION

In this paper, a new PWL memristor model with switches is proposed. This model compared with other published memristor models [15], [16] and after this comparison this model is verified. Although there are some differences among our model and other models due to the fact that our model is linear; however results are sufficiently compatible. Also, an equivalent memristor circuit model is proposed as a new memristor model. This circuit needs a negative resistor

for realizing as a physical circuit.

In here, we suggest an independent PWL memristor model from frequency. In our next studies we aim making a frequency dependent memristor model, improving an application for this model and research new equivalent circuit models with or without negative resistor will be our future studies.

Also this study made by linearized I-V characteristic of memristor. For future studies, M-V characteristic of memristor could be linearized and a new equivalent circuit may be derived.

Future improvements and new applications about memristor will be bringing physically realized memristor device to us. But for now, when we consider a physical memristor does not exist, usability of this model should not be overlooked for simulation modeling.

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