Device Model Extending from -40°C to -55°C Based on Evolutionary Strategy

Tengteng Lu*, Jinzhong Sun, Dong Li and Xiao Mo

***Abstract*—At design time, engineers want to simulate circuits at -55 °C. However, the value temperature of some device models provided by PDKs (process design kit) is as low as -40 °C. Simulating circuits at -55 °C with models will cause a certain deviation. In this paper, we propose the method to extend MOSFET (metal oxide semiconductor field effect transistor) model from -40 °C to -55 °C based on evolutionary strategy. I_{DS} at threshold voltages (Vth) and maximum I_{DS} of linear and saturation regions were acquired by simulating the MOSFET with a certain size under the PDK's useful temperature range. Then, we fitted data and obtained threshold voltages and maximum I_{DS} values corresponding to -55 °C. We used the evolutionary strategy algorithm to adjust some device model parameters so that simulated I_{DS} values are close to the respective fitting values. The fitness is the sum of the relative error of four values and becomes about 1/6 of the original value for the 1.8 V NMOS (N-Channel Metal-Oxide-Semiconductor) device. This method proposes a new idea to extend model temperature, which is beneficial to engineers' work.**

***Index Terms*—MOSFET, device model, optimization, evolutionary strategy**

I. Introduction

In some analog IC (integrated circuit) designs, the simulation at -40 °C cannot meet the demand, the engineer needs the simulation results at -55 °C, but the lowest useful temperature of PDKs (process design kits) is usually -40 °C. For example, the useful temperature for BSIM4 [1,2] (Berkeley Short-channel IGFET Model, used in the paper) is from -40 °C to 125 °C. The engineer often simulates circuits at -55 °C with the original model file to evaluate performance. This way will cause a certain deviation. Normally, the foundry cannot provide a lower temperature model of this process. Therefore, the engineer requires temperature extension of the device model.

Since there is no freeze-out or current overshoot phenomenon [3–6] that occurs at -55 °C, it is feasible to directly fine-tune the device BSIM4 model. Machine learning is widely used in IC design, such as logic synthesis, physical design, verification, testing, analog design, etc. [7]. There is little literature on the application of machine learning in device modeling. Some algorithms in the literature consume a lot of hardware resources or need big data support.

This paper applies the (1+1) evolutionary strategy (ES) [8] algorithm to adjust parameters and reduce errors. Compared with other algorithms, (1+1) ES requires smaller data and shorter time-consuming, which is very suitable for model optimization with a few parameters.

Structure of this paper: We first present in detail the steps of the ES algorithm in the model temperature extension. This part includes parameters introduction, error calculation, programming, and other information. We then apply the method in combination with the specific MOSFET (metal oxide semiconductor field effect transistor). The main part of this paper gives the effect of model temperature extension and discussion about the data. Finally, we explain possible challenges and future research directions.

II. Experiment and Method

N-Channel Metal-Oxide-Semiconductor (NMOS) and P-Channel Metal-Oxide-Semiconductor (PMOS) devices with different width and length ratios (W/L) are involved in the experiment. For 1.8 V MOSFET, transfer curves at different temperature in linear ($|V_{DS}|$ = 50 mV) and saturation ($|V_{DS}|$ = 1.8 V) regions are simulated, for 0.9 V MOSFET, transfer curves at different temperature in linear ($|V_{DS}|$ = 20 mV) and saturation ($|V_{DS}|$ = 0.9 V) regions are simulated, as shown in Fig. 1. And the temperate range is from -40 °C to 120 °C with an interval of 1 °C. In order to speed up the experiment, simultaneously simulate transfer curves in the linear and saturation regions in one circuit.

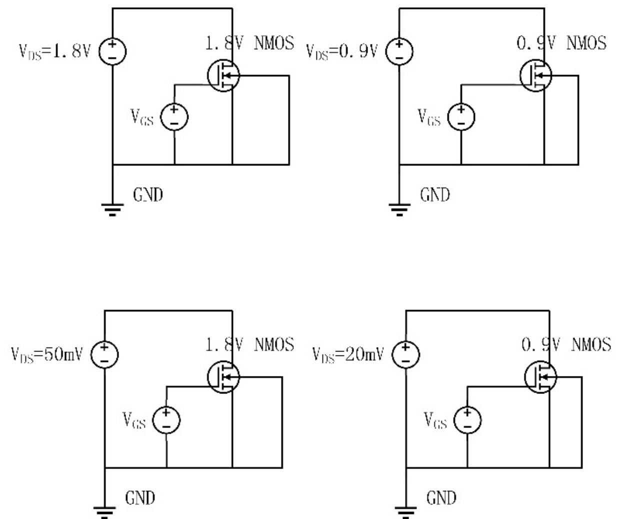

Fig. 1. Bias voltages setting for simulated transfer curves in the saturation and linear regions of 1.8 V NMOS device.

We have compiled the data of I_{DS} at Vth in the linear region (I_lin), the maximum current in the linear region (lin_Imax), the I_{DS} at Vth in the saturation region (I_sat), and the

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maximum current in the saturation region (sat_Imax). The Vth in the linear region (Vth_lin) and Vth in the saturation region (Vth_sat) are calculated with the following formula:

$$I_{DS}(\text{Vth}) = \frac{W}{L} \times 10nA \quad (1)$$

For instance, the W/L of the NMOS is 320nm/150nm, and the Vth is the value of V_{GS} when I_{DS} is 21.333 nA. Based on the value of I_{DS} (Vth), Vth_lin and Vth_sat are determined according to the simulation results.

A. Simulation Results

Fig. 2 and Fig. 3 display the simulation results of the transfer curve of linear and saturation regions of 0.9 V NMOS at different temperatures, the right axis corresponds to logarithmic value. Observing Fig. 2 and Fig. 3, Vth_sat and Vth_lin rise as the temperature decreases, so do sat_Imax and lin_Imax.

In addition, I_{DS}@V_{GS}=0 V decreases by about three orders with temperature dropping. Furthermore, the reduction of the subthreshold swing of the NMOS device is attributed to the temperature dropping. This change is conducive to digital logic design. However, larger I_{DS}@ V_{GS}=0.9 V at low temperatures is not conducive to power consumption limitation.

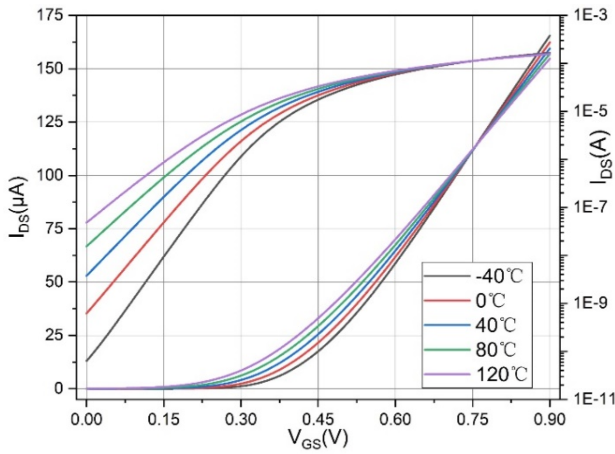

Fig. 2. Simulated transfer curve in the saturation region of 0.9 V NMOS with 200nm/30nm, showing five temperatures.

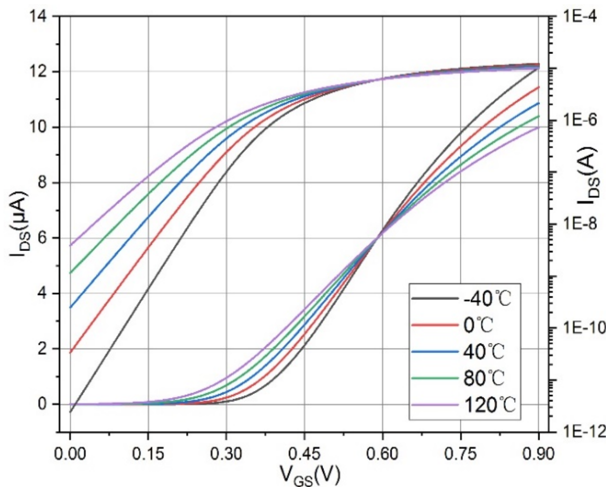

Fig. 3. Simulated transfer curve in the linear region of 0.9V NMOS with 200nm/30nm, showing five temperatures.

B. Data Fitting

Fig. 4 shows the simulated lin_Imax and sat_Imax under different temperatures, the right axis corresponds to sat_Imax. The second-order relationship between lin_Imax and temperature is more obvious than sat_Imax for NMOS. We perform second-order polynomial fitting to lin_Imax and sat_Imax, and calculate them at -55 °C based on the fitting results.

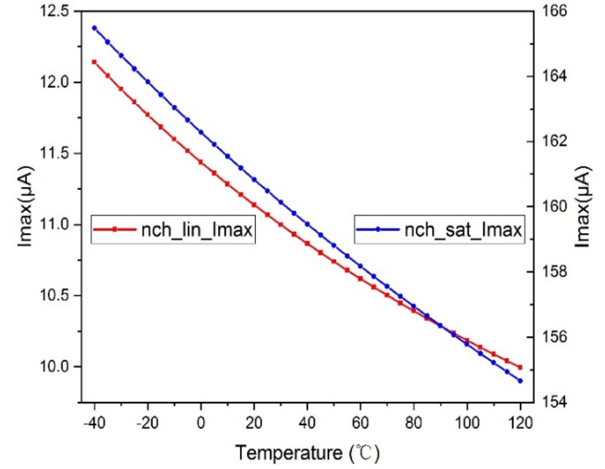

Fig. 4. Simulated lin_Imax and sat_Imax of 0.9 V NMOS with 200nm/30nm.

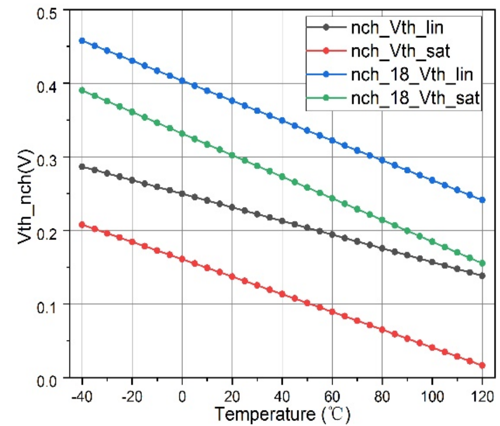

Fig. 5. Simulated Vth_lin and Vth_sat of 1.8 V and 0.9 V NMOS devices, temperature interval = 1°C, skip points = 5.

Fig. 5 and Fig. 6 show the simulated Vth_lin and Vth_sat under different temperatures for 0.9 V and 1.8 V MOSFET devices. We perform first-order polynomial fitting to Vth_lin and Vth_sat and calculate them at -55 °C based on the fitting results.

At the same time, we simulated Vth values in the linear and saturation regions with a common method for 1.8 V and 0.9 V MOSFET devices. In parametric analysis of spectre simulator, the temperature's linear step is also 1°C from -40 to 120 °C. Print the DC operating points of MOSFET devices, record the Vth value of MOSFET devices, and the simulation results are shown in Fig. 7. The left axis corresponds to NMOS devices, and the right axis corresponds to PMOS devices.

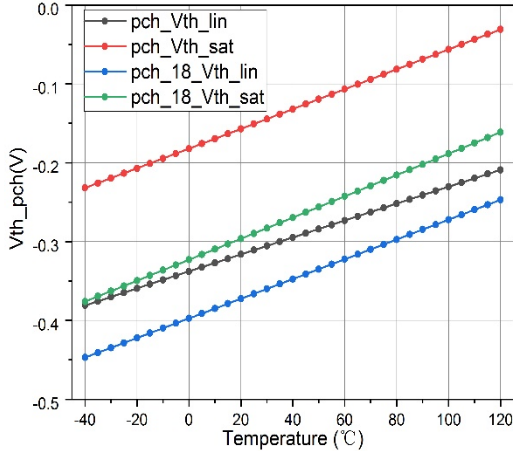

Fig. 6. Simulated Vth_lin and Vth_sat of 1.8 V and 0.9 V PMOS devices, temperature interval = 1°C, skip points = 5.

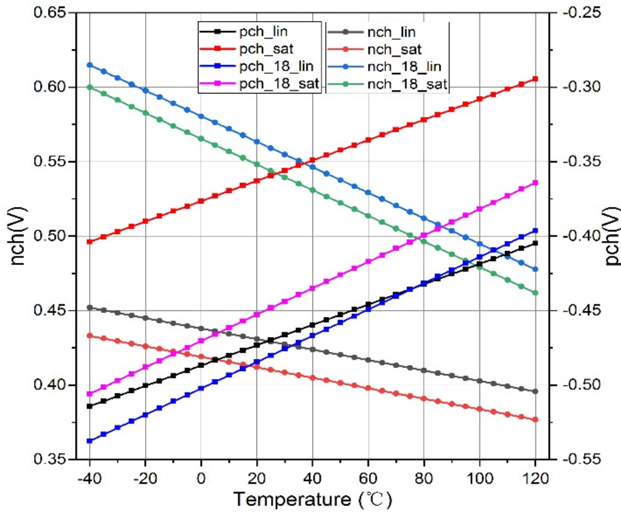

Fig. 7. Simulated Vth of 1.8 V and 0.9 V MOSFET devices, temperature interval = 1°C, skip points = 5.

Similar to Vth_lin and Vth_sat, the simulated Vth shows the same trend with temperature. Due to the drain induced barrier lowering (DIBL) effect, the Vth values in the saturation region are less than the Vth values in the saturation region for NMOS. This phenomenon is the same as |Vth| values of PMOS devices.

Comparing the Vth_lin and Vth_sat of 0.9 V and 1.8 V MOSFET devices in Fig. 5 and Fig. 6, the difference between Vth_lin and Vth_sat of 0.9 V MOS devices is less than 1.8 V MOS devices. We can also get a similar conclusion by comparing the data in Fig. 7. In addition, the gap between Vth_lin and Vth_sat of PMOS devices is larger than that of NMOS devices. PMOS devices are more sensitive to the DIBL effect than NMOS devices.

C. *Fitness*

We calculate the respective relative errors (RE) between the simulated value ($value_{simu}$) and the calculated value ($value_{cal}$) of I_lin, I_sat, lin_Imax, and sat_Imax under -55 °C. The fitness value is defined as the sum of four relative errors. The RE and fitness are calculated with the following formulas:

$$\mathrm{RE} = \frac{value_{simu} - value_{cal}}{value_{cal}} \quad (2)$$

$$\mathrm{fitness} = \mathrm{RE}_{\mathrm{I_lin}} + \mathrm{RE}_{\mathrm{I_sat}} + \mathrm{RE}_{\mathrm{lin_Imax}} + \mathrm{RE}_{\mathrm{sat_Imax}} \quad (3)$$

RE_{I_lin} is the relative error for simulated I_lin and calculated I_lin, RE_{I_sat} is the relative error for simulated I_sat and calculated I_sat, RE_{lin_Imax} is the relative error for simulated lin_Imax and calculated lin_Imax, and RE_{sat_Imax} is the relative error for simulated sat_Imax and calculated sat_Imax. A smaller fitness value means more accurate model parameters.

D. *ES Application*

We apply the (1+1) ES algorithm to the device model extension, and the brief flow chart is shown in Fig. 8. The adjusted parameters are vth0 (threshold voltage), vsat (saturation velocity at 25 °C), and u0 (low-field mobility at 25 °C) in BSIM4. Tnom (25 °C) is the temperature at which the model parameters are extracted. The version of the BSIM model in PDK is BSIM4 V4.5. Initial values are chosen in spectre model file. We use SKILL language to simulate the circuit, record I_lin, I_sat, lin_Imax, and sat_Imax, and call the external ES program with Python. The details of some steps are in the following.

Firstly, the initial fitness is calculated with initial parameter values. Then, the ES program randomly selects one of vth0, vsat, and u0, uses the following formula to perform mutation on it. The latter parameter value is in 0.99~1.01 times the former value and replaces the former value in the model file. This step uses an external Python script, and part of the code is shown in the appendix.

$$\mathrm{value}_{later} = \frac{random(-100,100)}{10000} \times \mathrm{value}_{former} \quad (4)$$

Where the random (-100, 100) randomly generates an integer value between -100 and 100. The value of the latter becomes between 0.99~1.01 times of the former iteration parameter value with Eq. (4).

Next, the SKILL script uses the new model file to simulate the linear and saturation region transfer curve and obtains the corresponding I_lin, I_sat, lin_Imax, and sat_Imax to calculate fitness. The external ES program called by the SKILL script calculates the latter fitness, compares the former fitness and the latter fitness, and selects the corresponding parameters with lower fitness as the parent of the next mutation.

We set the number of cycles in the SKILL script, and the program repeats the steps of mutation, simulation, calculation, and comparison of fitness. The program runs in the CentOS system, a 32-core 64-thread workstation. We put the frequently read and write files into the ramdisk to speed up the program. Due to the small scale of the circuit, the multi-core setting does not accelerate the circuit simulation. It takes less than 6 seconds to run a cycle of the program.

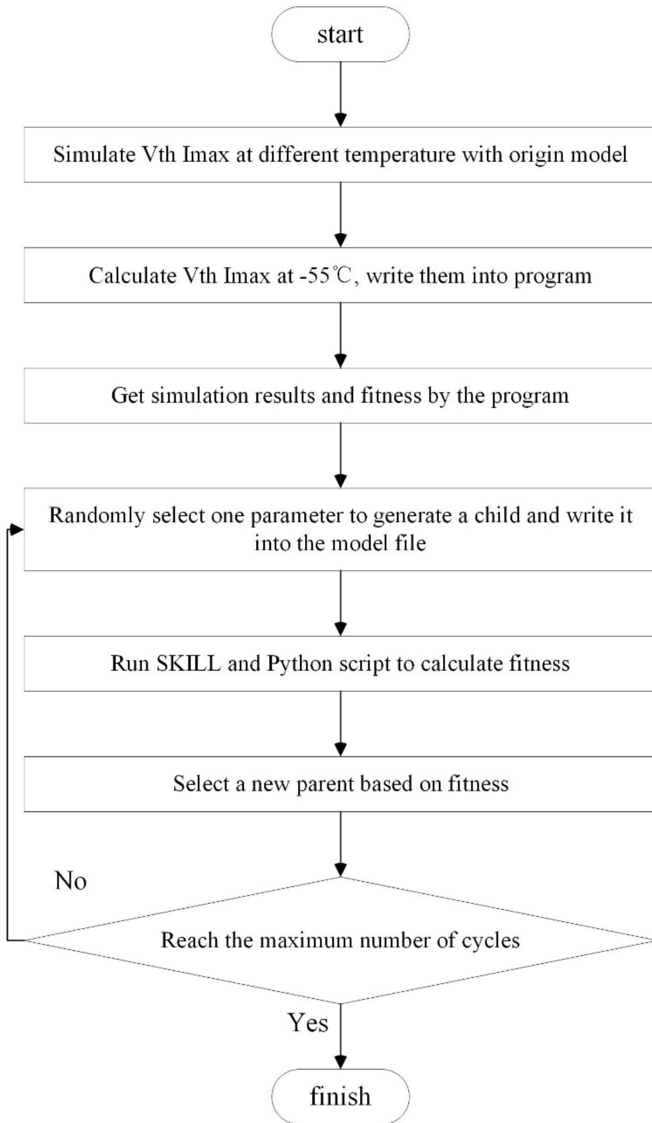

Fig. 8. Brief flow chart of the ES program.

III. Result And Discuss

We select the 1.8 V NMOS device with 320nm/150nm as the application object of the ES program, and the total iterative number is 10000. As shown in Fig. 9, the fitness is significantly reduced.

In Fig. 9, the fitness drops rapidly from the original value 3.615% to about 0.6%, and most fitness values are near 0.6%. By comparing all fitness values, the minimum fitness value is 0.571%, and in the later cycle, the model optimization effect is not obvious.

The first hundred cycles are shown in detail in Fig. 10. There are two very effective mutations in the first 20 cycles, and the fitness value drops sharply. Then the fitness value drops slightly as the number of cycles increases. We also apply the ES program to optimize the 1.8 V PMOS (W/L = 500nm/150nm), the corresponding optimization results are shown in Fig. 11 and Fig. 12.

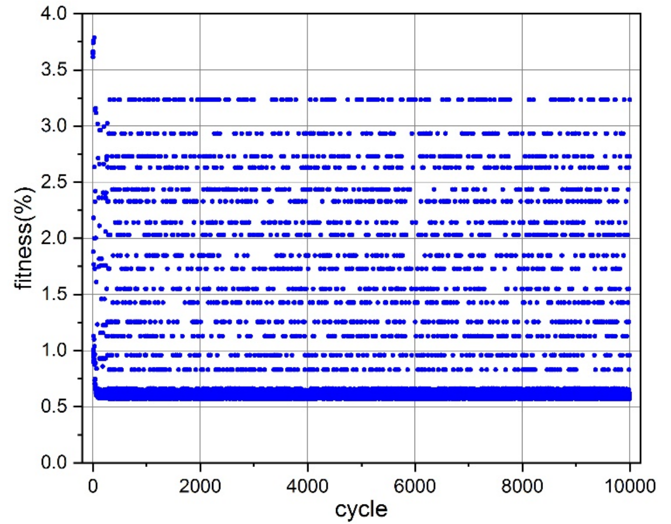

Fig. 9. Total 1.8 V NMOS model optimization result.

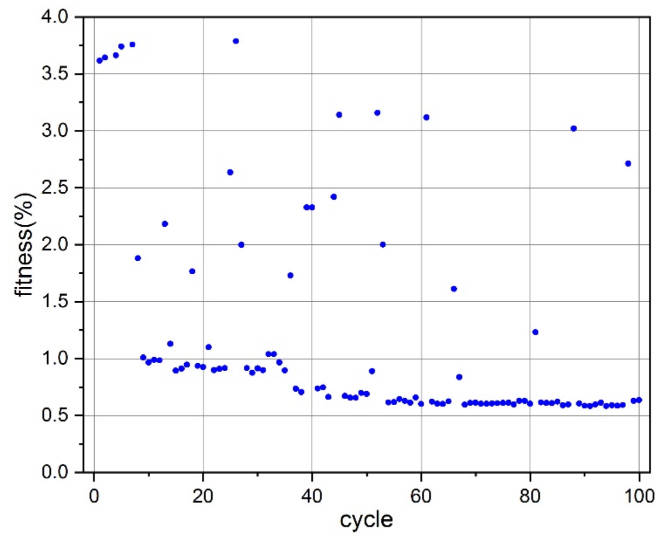

Fig. 10. The first hundred cycles model optimization result for the 1.8 V NMOS device.

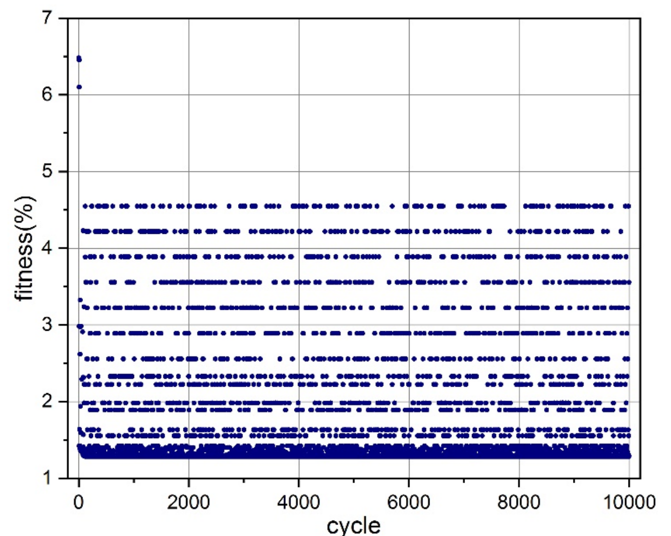

Fig. 11. Total 1.8 V PMOS model optimization result.

Similar to Fig. 9, breakpoint lines also appear in Fig. 11. This phenomenon may be caused by the limited number of decimal places of model parameters and the closeness of the former parameter and latter parameters.

The first hundred cycles are shown in detail in Fig. 12. There are several effective mutations in the first 20 cycles,

identical to Fig. 10. The optimization effect of 1.8 V PMOS is better than 1.8 V NMOS. 0.9 V NMOS (W/L = 200nm/30nm) and PMOS (W/L = 400nm/30nm) devices achieve similar optimization results, and related figures are included in the appendix.

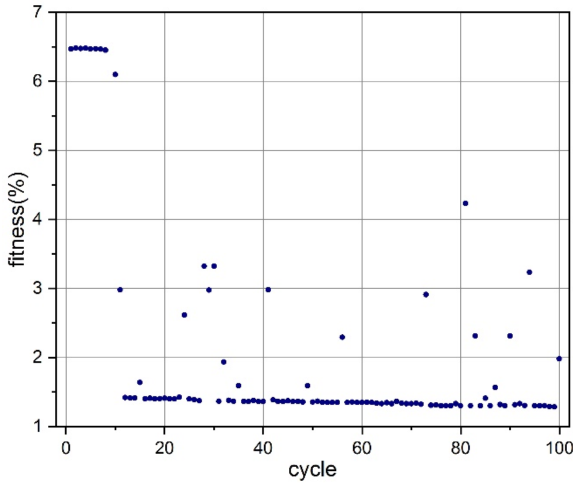

Fig. 12. The first hundred cycles model optimization result for the 1.8 V PMOS device.

IV. Conclusion

The (1+1) ES algorithm is applied to model optimization at -55 °C with SKILL and Python language. We have reduced the fitness value from 3.615% to 0.571% for the 1.8 V NMOS device, the fitness value from 6.468% to 1.284% for the 1.8V PMOS device, similar to 0.9 V devices. In this way, a more accurate device model at -55 °C can be obtained, which is convenient for engineers to simulate circuits performance at lower temperatures. In the future, devices such as capacitors and resistors will also be studied, and the degree of automation of the ES program will be improved. We will also consider applying the (μ, λ)- ES and (μ + λ)-ES algorithms to optimize the device model at -55 °C to see which is more efficient.

Appendix

The command of SKILL script to call external Python script is as follows: ipc1 = ipcBatchProcess (“python3 python script path &” “” “log file path”).

The command of SKILL script to read and save I_{DS} for 1.8 V NMOS under the setting bias voltages is as follows: fprintf (port1, “%10.1 5f\t%10.18f\t%10.15f\t%10.18f\n” value (i(“/M1/D” ?result “dc”) 1.8), value(i(“/M1/D” ?result “dc”) vth_lin), value(i(“/M2/D” ?result “dc”) 1.8), value(i(“/M2/D” ?result “dc”) vth_sat)). The value (waveform name 1.8) prints the value of the waveform for I_{DS} at V_{GS}=1.8 V.

The command of Python script to mutate parameter value is as follows (pop vector includes vth0, vsat, u0.):

i = random. Randint (0, 2)

a1 = pop[i]

pop[i] = a1 * (1 + random.randint(-100, 100)/10000).

Figs. A1 to A4 show the optimization results of 0.9 V NMOS and PMOS devices.

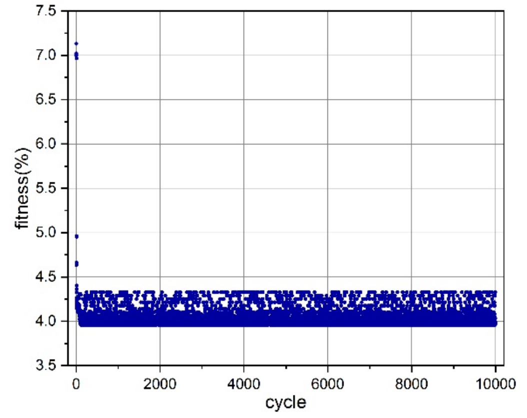

Fig. A1. Total 0.9 V NMOS model optimization result.

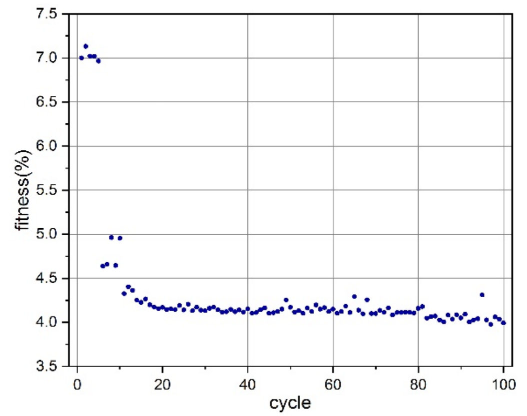

Fig. A2. The first hundred cycles model optimization result for the 0.9 V NMOS device.

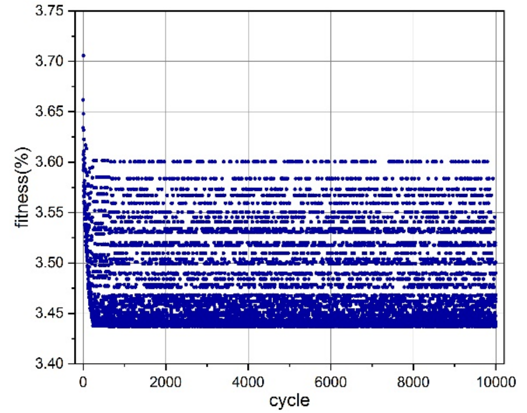

Fig. A3. Total 0.9 V PMOS model optimization result.

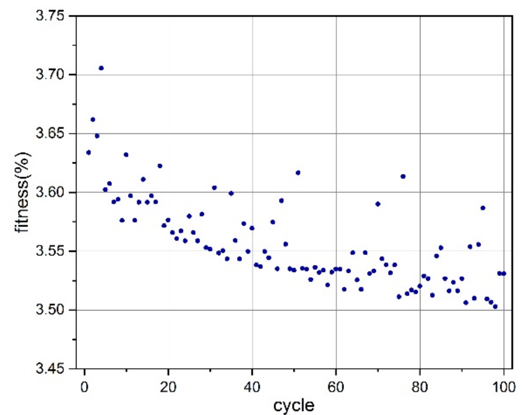

Fig. A4. The first hundred cycles model optimization result for the 0.9 V PMOS device.

Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

Tengteng Lu conducted the research; Xiao Mo analyzed the model file in PDK; Jinzhong Sun and Dong Li analyzed the data; Tengteng Lu wrote the paper; Xiao Mo provided the support for the SKILL script. All authors had approved the final version.

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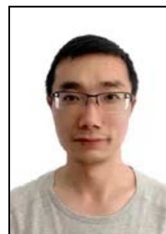

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