A Low Voltage Wideband CMOS Mixer with High Linearity

Hung-Che Wei

***Abstract*—A low voltage wideband CMOS down-conversion mixer is described. The g_m-boosted and the current-bleeding techniques are employed to improve the linearity of the proposed mixer. The mixer implemented by tsmc 0.18 μm CMOS process achieves maximum input third-order intercept point (IIP3) of 2.6 dBm, power conversion gains of 6.9 dB, and single side-band noise figure (SSB NF) 20.8 dB. The mixer operates over the entire 1.4–3.6 GHz LTE-advanced bands and consumes 6.5 mA of current from a 1.2 V power supply.**

***Index Terms*—4G, CMOS, LTE-advanced, linearity, low voltage, mixer**

I. Introduction

Due to the evolution of the modern communication, the demands for mobile internet access have grown in recent years significantly. there are several networks developed from short distance to long distance communication, such as wireless personal area network (WPAN), wireless local area network (WLAN), wireless metropolitan area network (WMAN), and wireless wide area network (WWAN). In the WMAN applications, there are two candidates for the next generation communication protocols. One is Worldwide Interoperability for Microwave Access (WiMAX) and the other is Long Term Evolution (LTE). A council called by the National Wireless Electronics Systems Testbed (N-WEST) of the U.S. National Institute of Standards and Technology initiates the 802.16 activities in August 1998. The effort was welcomed in IEEE 802, which led to the formation of the 802.16 Working Group (WG). The 802.16 WG has held weeklong meetings at least bimonthly since July 1999. The IEEE WG 802.16 on Broadband Wireless Access (BWA) Standards take charge of the evolution of 802.16 and the included WMAN air interface along with related revisions and standards[1]. Up to now, the mobile version IEEE 802.16m has been depicted for the fourth generation (4G) of cellular wireless standards.

LTE developed from the High-Speed Packet Access cellular standards is proposed by the 3rd Generation Partnership Project (3GPP). 3GPP consists of several international standards organization from the Europe, US, Japan, China, and South Korea. The LTE provides high data rates and wide coverage. LTE release 10 (LTE-advanced) is depicted in September 2009. The LTE-advanced operating bands are 698–960 MHz, 1710–2025 MHz, 2110–2200 MHz, 2500–2690 MHz and 3400–3600 MHz, respectively. Table I summarizes the comparison between the fixed IEEE 802.16m standard and the LTE-Advanced standard. Table I reveals WiMAX and LTE-Advanced technical specifications. [2].

TABLE I: WiMAX and LTE-Advanced Technical Specifications

	IEEE 802.16m	LTE-Advanced
Physical Layer	UL：OFDMA DL：OFDMA	UL： DFTS-OFDM DL：OFDMA
Duplex mode	TDD/FDD	TDD/FDD
Frequency Range (GHz)	0.45–3.8	0.7–3.6
User Mobility (km/h)	350	350
Modulation	QPSK, 16QAM, 64QAM	QPSK, 16QAM, 64QAM
Peak Data Rates (Mbps) (antennas)	UL：>200 DL：>350	UL：300 DL：1000
Channel Bandwidth (MHz)	5–40	1.4–20
VoIP capacity (users per sector/MHz)	>80 (FDD)	>30 (TDD)

Fig. 1 illustrates the direct-conversion receiver architecture. The direct-conversion receiver architecture includes band pass filters (BPFs), a low noise amplifier (LNA), mixers, a local oscillator (LO), low pass filters (LPFs), and amplifiers in the paths of receiving. The RF signal is received from the antenna, then amplified by the LNA. The LNA exhibits the signal amplification and low noise characteristic. The mixer demonstrates the function of frequency translation which converts the signal from high frequency to lower frequency. The signal to drive the local oscillator port of the mixers is generated by the LO. The BPFs/LPFs suppress the noise in the stopband and allow the signal at the passband pass through [3].

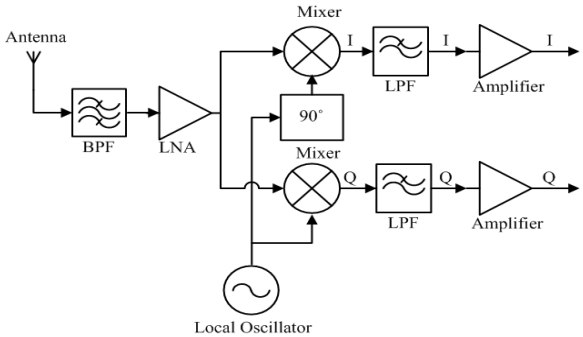

Fig. 1. Direct-conversion receiver architecture.

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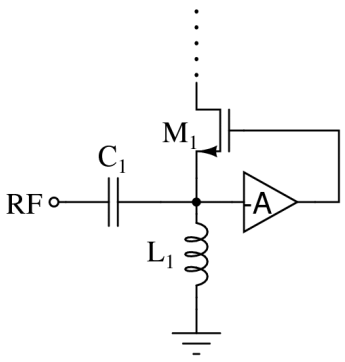

Fig. 2. g_m-boosted CG topology.

In the radio frequency (RF) receiver design, the linearity and noise of a receiver is calculated by

$$IIP3_{total} = \left(\frac{1}{IIP3_1} + \frac{A_1^2}{IIP3_2} + \frac{A_1^2 A_2^2 A_3^2}{IIP3_3} + \cdots \right) \quad (1)$$

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots \quad (2)$$

where A_n denotes the n-th loaded voltage gain, and $IIP3_n$ represents the IIP3 magnitude of the n-th stage, G_n denotes the n-th loaded power gain, and F_n represents the noise factor of the n-th stage. It shows the linearity of a receiver is dominated by the ones located following the first stage of the receiver. The overall noise performance of the receiver is affected by the first stage of the receiver such as LNA[4], [5]. The more $IIP3_n$ increases, the more $IIP3_{total}$ can be improved. IIP3 of a receiver is dominated by the subsequent circuits such as mixers in the receiver design.

II. Design Methodology of Mixers

As mentioned previously, the linearity of the mixer dominates the overall linearity of the receiver. So far, due to the nonlinear phenomenon of the transconductor stage, lots of methods have been proposed to improve the linearity of the mixer. A Gilbert cell mixer which adopts source degeneration connected to the sources of the transconductor stage is commonly revealed [6]. While employing the method depicted previously, trade-offs between the linearity and the conversion gain are considered. Another way to improve the linearity of a mixer is based on CMOS g_m Cell composed of the tanh functions [7], [8]. The transconductance linearization by multiple gated transistors compensation is depicted in [9],[10]. This architecture also leads to more power consumption due to the additional current path. The multiple gated transistors compensation also suffers from more passive devices for the compensated transistor. To adjust the threshold voltage (V_{th}) of the compensated transistor is a modified compensation method [11], but the negative bulk-source voltage will complicate the bias circuit design and power plan.

Fig.1 shows the gm-boosted common gate (CG) topology. M1 realizes a CG transistor and the inverting amplifier between gate and source of the CG transistor is employed for the g_m-boosted technique. Owing to the noisy inverting amplifier, g_m-boosted architecture can be realized by a capacitor. The CG architecture with the capacitor cross-coupling technique is suitable for the impedance matching to 50 Ω by the equivalent impedance and noise evaluation[12] –[14]

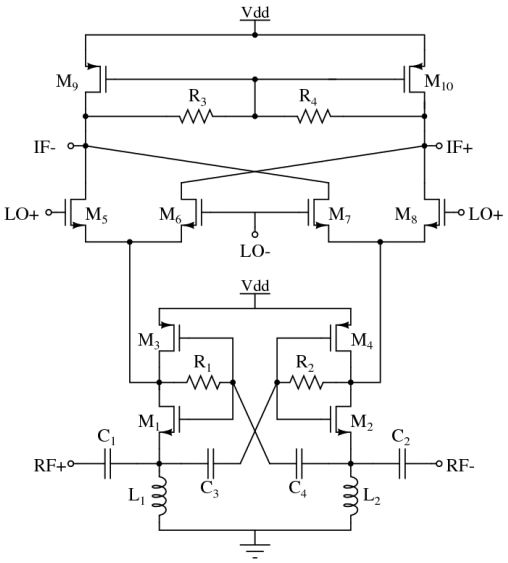

Fig. 3. Proposed mixer with the g_m-boosted current-bleeding transcoductor stage.

$$R_{in} = \frac{1}{g_m (1 + A)} \quad (2)$$

$$F = 1 + \frac{\gamma}{\alpha} + \frac{\delta\alpha}{5}\left(\frac{\omega_0}{\omega_T}\right)^2 \cong 1 + \frac{\gamma}{\alpha} \quad (3)$$

where α denotes a device-dependent parameter, and γ is a bias-dependent parameter. Due to the g_m-boosted CG and the capacitor cross-coupling technique, the CG and common source (CS) topologies can be realized in a g_m-boosted capacitor cross-coupling transconductor stage and the third-order intermodulation (IM3) of a transconductor stage can be suppressed. However, the overall gain of the topology is attenuated by the CG topology. The gain and linearity of the g_m-boosted CG can be improved by adopting the current-bleeding technique [15].

The proposed high-linearity mixer with a g_m-boosted current-bleeding transconductor stage is depicted in Fig. 2. The g_m-boosted current-bleeding transconductor stage consists of M_1–M_4, C_1–C_4, L_1–L_2 and R_1–R_2. M_1–M_4 and operate in the saturation region. C_1 and C_2 are the cross-coupling capacitors. M_3 and M_4 are the current-bleeding transistors and improve the conversion gain and IIP3 of the proposed mixer. R_1 and R_2 are the wideband input matching network of RF port. Due to the feedback matching network of the RF port, the RF port does not require the external bias voltage. The g_m-boosted current-bleeding transconductor stage converts the input RF voltage signals into small output current signals to the commutating stage. The commutating stage is often driven by the power from LO in the RF front-end. The commutating stage which consists of M_5–M_8 acts as ideal switches when the input LO power is large. If the LO power is small, the commutating stage acts as an amplifier. The DC operation point and the aspect ratio of the commutating stage will

influence the requirement of the driven LO power. The transistors are biased in the boundary between the saturation region and the triode region to make M_5–M_8 act as ideal switches with lower driven power. The RF signal is injected from the source of M_5–M_8, then the IF current signal is down-converted by the commutating stage with the multiplied function. The load stage consisted of M_9, M_{10}, R_3 and R_4 translates the down-converted current signal into the voltage signal. R_1 and R_2 can provide output impedance and M_9 and M_{10} can provide appropriate voltage swing headroom. The proposed g_m-boosted current-bleeding transconductor stage compensates the IM3 phenomenon by adjusting the bleeding current and cross-coupling capacitors. However, the bleeding current also increases the power consumption of the mixer. In the mixer design, the trade-offs between IIP3, conversion gain and NF are the main design considerations. Due to the NF of the receiver is dominated by the NF of the LNA, the proposed mixer can be optimized in the aspects of linearity and conversion gain.

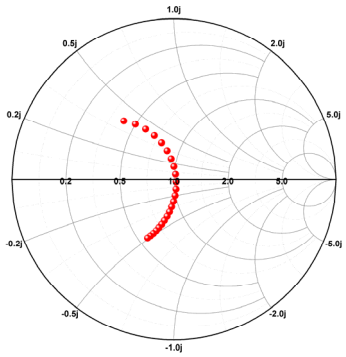

Fig. 4. RL of the RF port on smith chart.

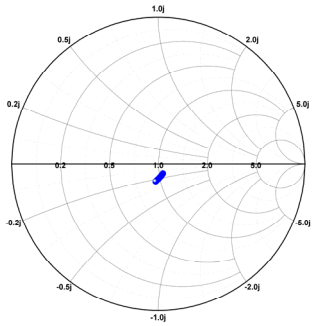

Fig. 5. RL of the IF port on smith chart.

III. Simulation Results

The simulator for the circuit simulation is Agilent Advance Design System (ADS) 2009. The proposed mixer is realized by tsmc 0.18 μm Mixed Signal CMOS RF model. The RF is from 1.4 GHz to 3.6 GHz in the simulation of the proposed mixer, Due to the fixed IF of 10 MHz, the LO frequency is from 1.39 GHz to 3.59 GHz. The active current of the mixeris about 6.5 mA from a 1.2 V supply voltage. The three terminals of RF, LO and IF ports will be matched to 50Ω for optimizing the mixer. The Return loss (RL) of RF port on Smith chart is illustrated in Fig.4. The RL of the RF port reveals the matched state. The red circles are the impedance from 1.4 GHz to 3.6 GHz. Although the RL of RF is more than –10 dBm from 1.4–1.5 GHz, the proposed mixer can still operate appropriately. The simulation results of the RL of the IF port on Smith chart are illustrated in Fig. 5. The points denote the impedance from 5 MHz to 100 MHz. As shown in Fig. 6, the maximum conversion gain reached the peak value of 8.3 dB at the RF of 2.3 GHz when the LO power is –5 dBm. To optimize the overall performance of the proposed mixer, the LO power is –8 dBm The conversion gain of the proposed mixer is 4.3–6.9 dB and the SSB NF is 20.8–23.2dB.

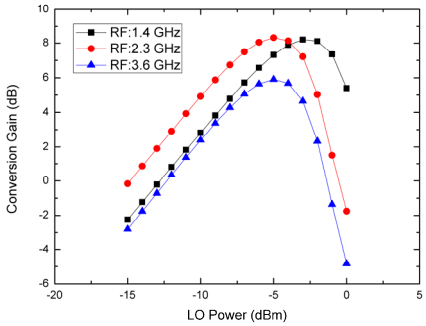

Fig. 6. Conversion gain versus LO power at different frequencies.

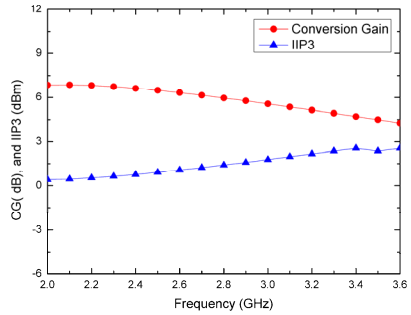

Fig. 7. Conversion gain (CG) and IIP3 versus RF.

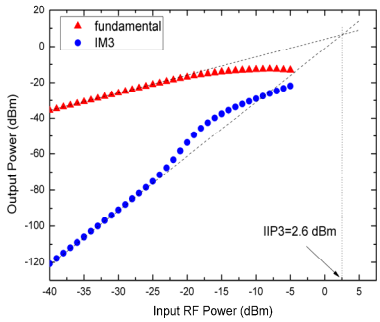

Fig. 8. IIP3 characteristic at 3.6 GHz.

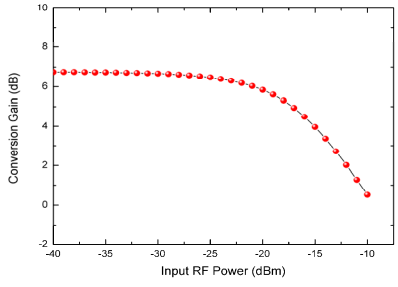

Fig. 9. P_{-1dB} characteristic at 2.4 GHz.

IIP3 of the mixer is calculated by using a two-tone testing. The frequency spacing in the two-tone test is set to be 300 kHz which is the channel spacing in a LTE-advanced system. Fig. 7 illustrates CG and IIP3 versus RF. The conversion gains are 4.3–6.9 dB. The extrapolation plot of IIP3 is illustrated in Fig. 8 and the maximum measured IIP3 achieves 2.6 dBm at 3.6 GHz and the minimum IIP3 is –0.6 dBm at 1.4 GHz. The simulation results of P_{-1dB} is shown in Fig. 9, which achieves – 13 dBm alongside the various RF input power at 2.4 GHz. The simulation results of other mixers are compared by the same design consideration in optimizing the linearity. Table II summarizes the simulation results of the proposed mixer. The proposed mixer reveals excellent properties of linearity and power consumption.

TABLE II: PERFORMANCE SUMMARY OF MIXERS

	Ref.		This work
	[16]	[17]	
Process (μm)	0.18	0.18	0.18
Supply Voltage (V)	1.8	1.8	1.2
f_{RF} (GHz)	1.9	2.4	1.4–3.6
f_{LO} (GHz)	1.95	2.25	1.39–3.59
Current consumption (mA)	23.56	14.5	6.5
LO Power (dBm)	–1.2	4	–8
IIP3 (dBm)	20.45	8.6	–0.5–2.6
P-1dB (dBm)	12.8	1	–12.9––13.9
Conversion Gain (dB)	1.65	–5.3	4.3–6.9
SSB Noise Figure (dB)	17.2	17.5	20.8–23.2

IV. CONCLUSION

A 1.2 V wideband high-linearity CMOS mixer with the g_m-boosted current-bleeding transcondutor stage is presented. The proposed mixer operates at the RF of 1.4–3.6 GHz, the LO frequency of 1.39–3.59 GHz, and IF of 10 MHz, respectively. The mixer is realized by adopting the linearity compensation method based on the g_m-boosted current-bleeding transconductor. Both of the conversion gain and the linearity are improved. The mixer consumes 7.8 mW from a 1.2 V power supply. The simulation results of the proposed mixer exhibits maximum power conversion gain of 6.9 dB, IIP3 of 2.6 dBm, and single side-band noise figure of 20.8 dB. The proposed mixer reveals high conversion gain and IIP3 and is suitable for LTE-advanced applications.

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