

# Frequency-Dependent Description of the Thermal Energy Inputs in Each Layer of a Semiconductor by Using Bode Diagrams

M. Richter, O. Koller, M. Kopp, R. Schroth, and J. Lutz

**Abstract**—Power semiconductors operate at different loads with different repetitive frequencies depending on each application. The resultant power loss of a semiconductor can be dissipated as a heat flow or absorbed. In this paper, the thermal path is described frequency-dependent by the power loss input to the thermal mass.

The thermal path is defined through the packaging and described by a Cauer model. It consists of thermal resistors and capacitors which depend on the material and which can be realized through a continuous fraction element for each layer. This arrangement causes a frequency dependency of the transmission behavior of the package, which is shown in this paper by using the Bode diagram. Two different systems are described; a diode and a DBC module. The frequency-dependent description using the Bode diagram makes it possible to calculate the energy input into individual layers. Thereby the load of the layer is determined as a function of the amplitude and frequency of the input power. The frequency analysis of the input signal in combination with the material-dependent Cauer model allows prediction of the critical layers.

**Index Terms**—Power semiconductor, thermal energy inputs, description of the thermal path, frequency-dependent layer composite, Bode diagram.

## I. INTRODUCTION

The thermal connection of a power semiconductor on the heat sink is currently investigated in many research institutes and research facilities [1]–[3]. Each layer of the thermal connection has a number of functions in order to ensure the operation of the power semiconductor. The main functions are:

- 1) dissipation of the introduced power loss
- 2) ensuring a mechanical connection
- 3) ensuring an electrical contact

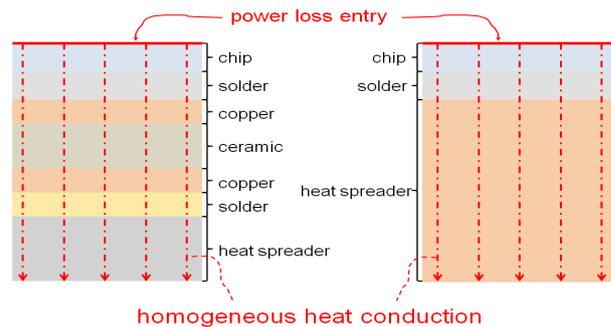


Fig. 1. Layer composite of a DBC module left (schematically taken from [5]) and of a diode right.

Power electronic devices are mainly used as switches and are subject to high cyclic stress, which manifests itself in the form of a power loss entry in the junction. This will dissipate through each layer of the module and, dependant on the material layer, will either be absorbed or conducted. Absorption of thermal energy may cause a structural change of the material, which leads to material fatigue. The cyclic variation of the material promotes all damage mechanisms until failure. In order to make better conclusions on the time to failure, a frequency dependent consideration of the power inputs is described in this paper.

## II. COMPOSITE LAYER

The composite layer of a power semiconductor includes all layers that will conduct the heat flow along the cooling path starting at the power input and ending at the thermal mass (shown schematically in Fig. 1). The thermal mass is generally assumed to be the potential of the surrounding air or the cooling medium.

### A. Physical Based Equivalent Circuit

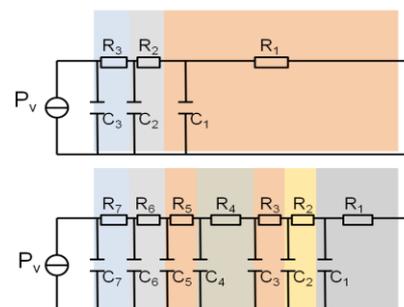


Fig. 2. The Cauer model of a diode (top) and of a DBC module (bottom).

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As described in [4], for the case that no other sources of heat are present within a layer, the temporal change of temperature is described by the homogeneous heat conduction equation in differential form:

$$\frac{\partial \vartheta(x,t)}{\partial t} = \frac{\lambda}{\rho c} \frac{\partial^2}{\partial x^2} \vartheta(x,t) \quad (1)$$

where  $\vartheta$  is the temperature,  $x$  the path length,  $t$  the time,  $\lambda$  the thermal conductivity,  $\rho$  the density and  $c$  the specific heat capacity.

According to [4], the differential equation for the induction-free line, the following analogy to the heat conduction is obtained:

$$\frac{\partial \varphi(x,t)}{\partial t} = \frac{1}{R'C'} \frac{\partial^2}{\partial x^2} \varphi(x,t) \quad (2)$$

where  $R'$  and  $C'$  are the resistive and capacitive behavior of a line or cable. Substitution of the density  $\rho = m/(Al)$  into equation (1) together with the relationships results in a complete analogy between the temperature and the electrical potential. From this it can be concluded that the thermal behavior of a layer can be related to the electrical equivalent circuit. The heat conduction through a plurality of layers is therefore described by a concatenation of multiple unit lengths, known as the Caer model [6].

$$C_{th} = m c \quad (3)$$

$$R_{th} = \frac{l}{\lambda A} \quad (4)$$

### B. Caer Model

The thermal behavior can be represented by the Caer model to an equivalent electrical circuit using resistors and capacitors (Fig. 2). The temperature dependence is seen as a result of the power input. The thermal impedance  $Z_{thn}$  of a Caer model can be expressed (see [7]) as:

$$Z_{thn} = \frac{1}{sC_n + \frac{1}{R_n + Z_{thn-1}}} \quad (5)$$

Establishing the impedance, it has proven to be beneficial to index the layer structure in the direction opposing the thermal flux.

### C. Material Properties and Layer Structure

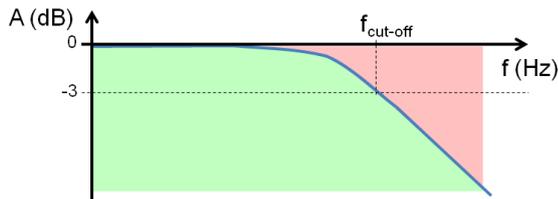


Fig. 3. Interpretation of the amplitude response of a single layer.

In this paper two different power semiconductor modules will be examined; first a standard DBC module (MOSFET) and secondly a diode (pin diode). At this stage, only the main path will be considered under the condition of thermal homogeneity. Other thermal phenomena such as spreading and edge convection are neglected. The material properties are shown in Table I.

TABLE I: MATERIAL PROPERTIES

Layer	DBC module		diode	
	$C_{th}(Ws/K)$	$R_{th}(K/W)$	$C_{th}(Ws/K)$	$R_{th}(K/W)$
heat spreader	11.5000	1.9700	0.4231	1.091
solder	0.0060	0.7380		
copper	0.0470	0.0177		
ceramic	0.1370	0.4610		
copper	0.0470	0.0177		
solder	0.0081	0.0440	0.0009	0.067
chip	0.0180	0.0520	0.0042	0.099

### III. SYSTEM ORIENTED DESCRIPTION OF A LAYER

The power ratio between the output power  $P_{v_{n,j}}$  and input power  $P_{v_n}$  for a layer is called the transfer function  $G_{sn}$ .

$$\frac{P_{v_{n-1}}}{P_{v_n}} = G_{s_n} \quad (6)$$

$G_s$  can be established through a description of the thermal conductivity with an equivalent electrical circuit diagram by using the current divider rule. The transfer function word by the Laplace variable  $s$  of a layer without subsequent layers is shown in [7]:

$$G_{s_1} = \frac{1}{C_1 R_1} \frac{1}{s + \frac{1}{C_1 R_1}} \quad (7)$$

#### A. Bode Diagram of Individual Layers

The Bode diagram, in addition to other forms of data representation such as the Nyquist diagram, is particularly suitable for visualization. It shows the dynamics of the system over the frequency. For this, the amplitude and the phase response are required. The phase response, as a temporal displacement between power input and output, describes the frequency-dependent inertia of the system.

The amplitude response is interpreted as a power loss damping, thus the surface below the curve is a measure of the dissipated power (in Fig. 3, the green shaded area). The area between  $y = 0$  and above the curve is a measure of the absorbed power (in Fig. 3, the red shaded area).

The Bode diagrams from individual layers of the DBC module and the diode are shown in Fig. 4. Depending on the application, these diagrams can illustrate some initial conclusions regarding the power absorption. The cut-off frequencies of individual layers are well within the range of the actual load cycles and can therefore be regarded as critical.

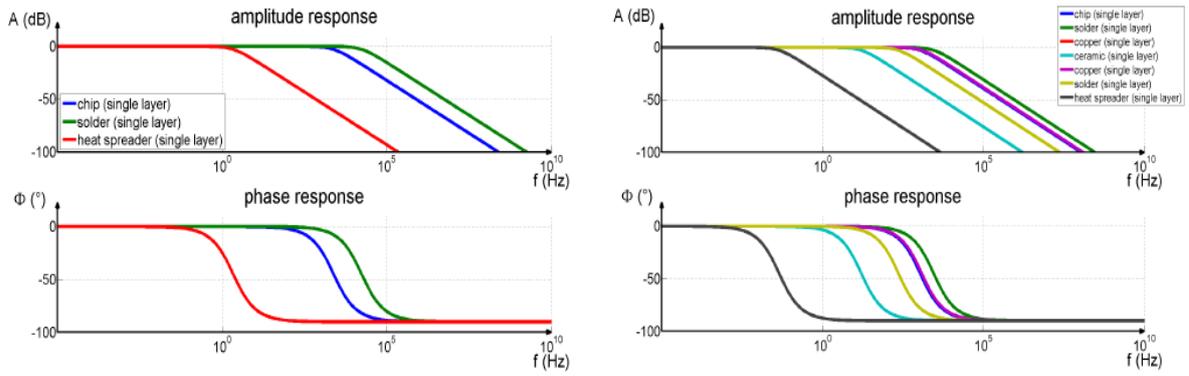


Fig. 4. Bode diagram of single layers of a diode (left) and of a DBC module (right).

#### IV. SYSTEM ORIENTED DESCRIPTION OF A LAYER IN THE LAYER COMPOSITE

The transfer function of a layer, as shown in the previous chapter, has only one cut-off frequency. Through the assembly of further layers, the thermal resistance increases and the frequency response of one layer changes. If the transfer function  $G_s$  of one layer is prepared according to eq. 6 for only one additional layer in the assembly, two poles (denominator zeros) are formed (eq. 8). They may be purely real, double root or conjugate complex. According to [8] the conjugate complex pole can produce overshoots that must be avoided, because they can lead to instability of the system.

$$G_{s,2} = \frac{C_1 R_1 s + 1}{C_1 C_2 R_1 R_2 s^2 + (C_1 R_1 + C_2 R_2 + C_2 R_1) s + 1} \quad (8)$$

If there are more additional layers, the denominator and numerator polynomial very quickly becomes lengthy and complicated. For this reason they are not shown here.

##### A. Layer Dependent Bode Diagram in the Composite

Fig. 5 shows the Bode diagrams of all layers in a diode and the effect of their composite layers. The Fig. 6 also includes the Bode diagrams from the DBC module. These transfer functions of layers have more poles and zeros than the  $G_s$  without subsequent layers. Considering the amplitude response (in Fig. 5 plotted logarithmically) and interpreting the power transmission with the manner indicated in Fig. 3, it

is apparent that the surface of the absorbed power (red area in Fig. 3) increases. According to this, more power is absorbed in the layer and the energy input is greater.

#### V. QUANTIFYING THE AMPLITUDE RESPONSE DISPLACEMENT

The additional power entry can be calculated as an integral area between the single layer amplitude curve (shown in Fig. 4) and the amplitude curve of a layer in its composite (shown in Fig. 5). The integral area of two functions is defined as a difference of both curves. The general formula is given as

$$\Delta A = \int_0^{\infty} (a_1(f) - a_n(f)) df \quad (9)$$

This integral calculates the area between the two curves and returns only one value. To see the change depending on the frequency, the difference of both curves is needed.

$$\Delta a(f) = a_1(f) - a_n(f) \quad (10)$$

The amplitude response difference is shown in Fig. 7. This figure displays the effect of the layer composite on the dynamic behavior of each layer. For example, the power input of the Si layer in the analyzed diode increases by about 4 dB at a frequency of 6000 Hz (max. point Fig. 7) compared to the single chip layer without following layers. In Table II the main properties of the layer composite influence on each layer are shown.

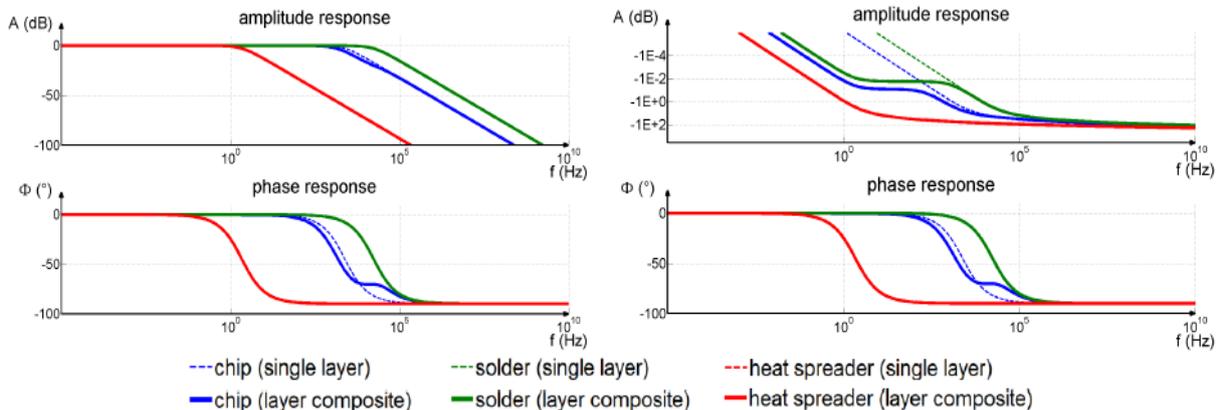


Fig. 5. Bode diagram of layers in a composite of a diode (left) and a logarithmic view of the amplitude response (right).

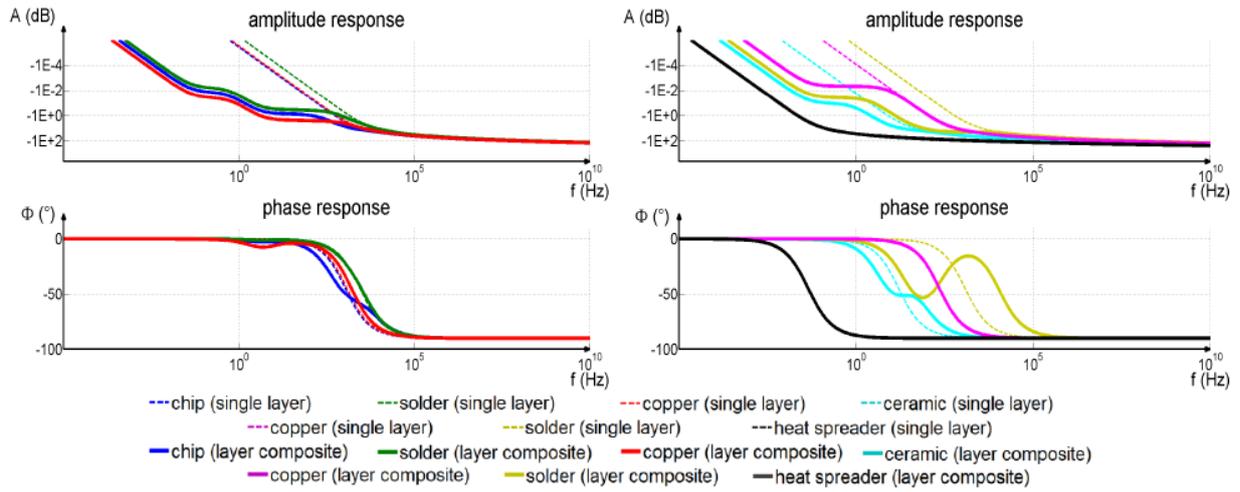


Fig. 6. Logarithmic view of Bode diagrams from layers in a composite of a DBC module (left, first three layers) and right the amplitude response of the next four layers.

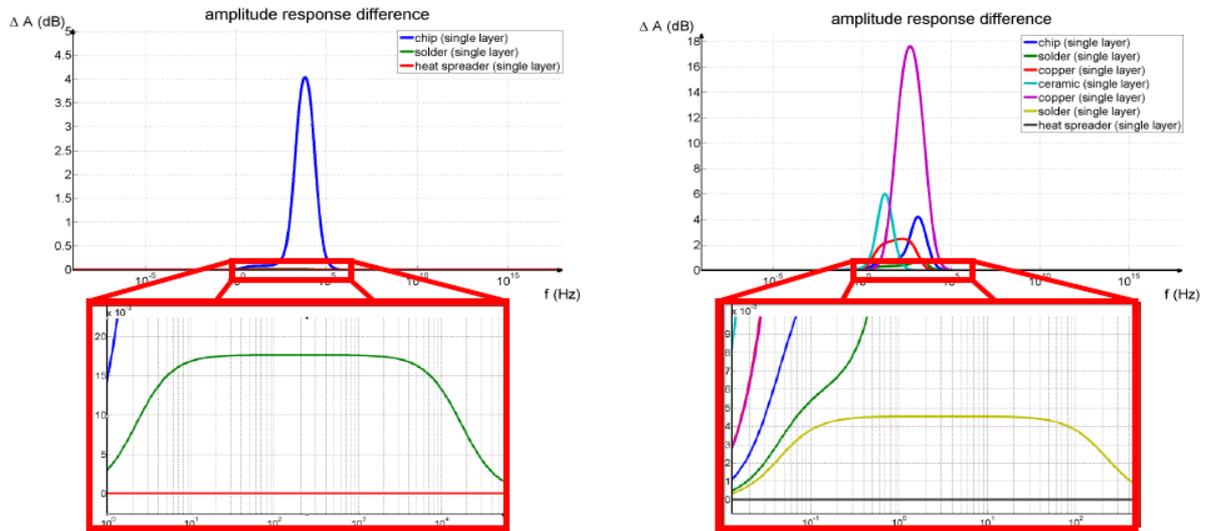


Fig. 7. Amplitude response difference of a diode (left) and a DBC module (right).

TABLE II: PROPERTIES OF THE LAYER COMPOSITE INFLUENCE ON EACH LAYER FROM A DBC MODULE AND A DIODE

Layer	DBC module			diode		
	$\Delta A$ (dB/s)	max. additional power entry (dB)	frequency of max. power entry (Hz)	$\Delta A$ (dB/s)	max. additional power entry (dB)	frequency of max. power entry (Hz)
heat spreader	0	-	-	0	-	-
solder	0.621	0.0045	3.065			
copper	1190	17.61	536.7			
ceramic	254.4	6.03	19.83			
copper	224.2	2.482	224.6			
solder	60.94	0.909	1751	2.553	0.017	196.3
chip	232.3	4.206	1365	202.1	4.043	6469

To rate the layer structure for a semiconductor it is necessary to know the operating point or the operating frequency. Especially for the layout of a layer composite, such as layer thickness and material, it is helpful to know the influence of the dynamic behavior of each layer according to the following layers.

## VI. CONCLUSION

This paper describes a new method in which the changes in

the dynamic behavior of a layer caused by its composite can be analyzed in the frequency domain by using a Bode diagram. Depending on the operating frequency, this may necessitate changes during the layout phase of the semiconductor module. The surface integral  $\Delta A$  is a measure of the overall change and should be kept small. In particular, it should be ensured that the maximum of the  $\Delta A(f)$  is not at the same location as the operating frequency.

Using a frequency-dependent treatment, the change of the energy input of each layer can be described with respect to the

layer structure and the applied power. The shape of the cyclic loading affects the reliability of the component and therefore can be used for the consideration of the suitability of the layered composite with known load cycles. This influences the choice of the solder and the assessment of the electrical contact application, such as bonding or soldering.

In further investigations, design rules can be derived from the knowledge gained to optimize the thermal behavior of layer composite.

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