

Modeling of Short Channel MOSFET Devices and Analysis of Design Aspects for Power Optimisation

Kiran Agarwal Gupta, Dinesh K. Anvekar, and Venkateswarlu V.

Abstract—The advancement in silicon material processes technology in the manufacture of 45nm MOSFET has extended Moore's Law for some more years. Low power CMOS circuit design has become a challenge due to variations in design parameters caused as a result of short channel effects at deep submicron levels for technology nodes below 1µm. In this paper, we have analyzed the design aspects for short channel devices by method of transistor modeling and further simulations have been carried out using Virtuoso cadence Simulator. The technology nodes considered here are 180nm and 45nm technology since fabrication of 180nm uses conventional process technology and 45nm uses new innovations in process technology. The aim of this paper is to bring out parameter variability issues related to different process technologies and find solutions for power optimization at design level for CMOS circuits.

Index Terms—Short channel effects, CMOS, technology node; Threshold variation, low power, scaling.

I. INTRODUCTION

The never ending demand of miniaturization and low power has led to a new dimension in Integrated circuit Era-Deep Submicron technology and Nano Technology. But continuous shrinking in channel length has posed new challenges such as short channel effects, high leakage current and static power dissipation. As the transistor scaling continued, fundamental limits of sizing of gate insulator reached and transistor could not be scaled any further. Intel's 45nm CMOS technology is the first in the world to replace polysilicon to new high-k dielectric material. Gordon Moore has called "the biggest change in transistor technology since 1960s" [1]. The insulating material silicon oxide between the transistor's gate and the channel was replaced by hafnium oxide which reduced the leakage current between gate and the channel. But other leakage currents still dominate the chips at smaller nodes giving rise to a need of fundamental change of transistor structure. The other two ways to control the leakage of short channel transistors are ultrathin body silicon-on-insulator or UTB SOI and FinFET or Tri-Gate

devices [2]. Though designers are working on 30 nm and 20 nm nodes, it will require new fabrication techniques and has its own limitations and challenges to face ahead. Thus the low power circuit design for high performance can be still explored for existing foundries of 180 nm- 45 nm technology nodes.

In this paper we have presented simulation results of 180 nm and 45 nm nMOS transistor. Here we have studied and compared short channel Effects (SCE) and other design problems like leakage currents for both the technology nodes. We have also explored the limitations and proposed the possibilities of using these SCE for design of low power CMOS circuits.

This paper is divided into four sections. Section I gives the introduction to the latest scaling trends and the advancement in process technology to overcome SCE. Section II gives a brief overview of the power dissipation concerns for short channel devices. In section III we have presented the simulation results of 180nm and 45nm devices for study of transistor behavior with respect to sub threshold currents and OFF state leakage currents. Section IV presents the threshold voltage model for short channel devices and experimental results for comparison of both the technologies for SCE and its impact on V_{th} . Last section is the conclusion of the work.

II. STATIC POWER DISSIPATION DUE TO SCALING OF DEVICES

Designing of a CMOS circuit above deep submicron levels involved a trade-off between chip area, performance and dynamic power dissipation. Now, deep submicron level circuit designs also have to deal with new design issues called as short channel effects (SCE) and this has led to innovation of new design techniques both at all levels of abstraction from floor planning to device fabrication.

A. Power Dissipation in Short Channel Devices

As seen from (1) and (2), the performance and operating speed of analog or digital circuits is directly dependent on the supply voltage [3].

$$P_{dyn} = \alpha C_L V_{DD}^2 f_o \quad (1)$$

where,

- α = Switching activity of transistors
- C_L = Load capacitance
- V_{DD} = Supply voltage
- F = Operating frequency

P_{dyn} is the power dissipation when the circuit is working or

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in active mode and P_{static} is the power dissipation when the circuit is not in active mode. P_{dyn} results from charging and discharging of the capacitors due to switching activity of the transistor. But continuous scaling of Metal Oxide Semiconductor field effect transistors (MOSFETs) to deep submicron levels has delivered lesser area and low capacitance effects leading to negligible dynamic power dissipation. Also miniaturization has led to the performance gain, cost reduction, and portability for semiconductor chip applications.

B. Static Power Dissipation in Short Channel Devices

Static power dissipation is an important factor to be considered for deep submicron chips since it dominates deep submicron devices and increases with shrinking technology node. Equation (2) represents static power dissipation.

$$P_{static} = I_{Leakage} V_{DD} \quad (2)$$

where $I_{leakage}$ is the leakage current flowing through different nodes of the circuit in inactive state. The main cause of leakage currents for short channel devices is the non-uniform doping under the gate region and thinner oxide layer which cause more leakages such as subthreshold current leakage, tunneling gate leakage current and OFF state leakage current. Since portable devices and hand-held devices remain in standby mode for longer duration, the stand-by leakage current has become the major design issue. Also, practically it has been observed that decreasing supply voltages for short channel devices has not helped in overall power consumption in circuits. This is due to the fact that at shorter channels dynamic power becomes negligible, but due to rise in static leakage currents, static power dissipation raises making power dissipation almost equal for the CMOS circuits both in ON and OFF states of the device.

C. Regions of Operation in MOSFET

The general behavior of a short channel MOSFET can be explained with Fig.1. The overall operation of a MOSFET has been classified into four regions based on variation of ON resistance R_{out} as V_{DS} is increased. The first region of operation is triode or linear region. This region represents channel current when V_{DS} is less than V_{gs} and the output resistance R_{out} is low.

• Drain characteristics

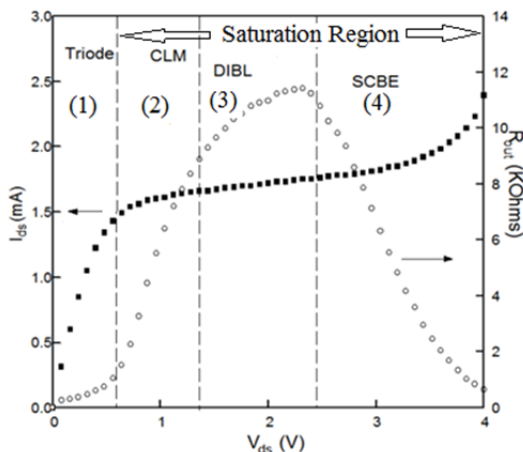


Fig. 1. MOSFET behavior showing R_{out} and regions of operation [4]

The region of operation above threshold voltage, where channel current becomes constant is called as saturation region which can be further divided in three parts- region 2, region 3 and region 4. In the second region channel current has weaker dependence on drain voltage and is dominated by channel length modulation. Region 3 is dominated by DIBL effect wherein threshold voltage has a strong dependence on drain voltage leading to unpredicted variations in circuit performance and has maximum R_{out} . The fourth region is called as Substrate current induced body effect (SCBE) which reduces R_{out} as shown in figure. When drain voltage is very large (Electric field $> 0.1\text{mV/cm}$), some electrons coming from source will be energetic enough to cause impact ionization increasing substrate current. Thus, I_{sub} will increase exponentially with drain voltage causing an increase in the drain current and this is also called as impact ionizations and this state of electrons is termed as “HOT” electrons.

III. OPERATION OF MOSFETs IN SUBTHRESHOLD REGION

The region of operation below threshold voltage is called as subthreshold region of operation. This region forms very important part of this study as most of the leakage currents flow in this region causing static power dissipation in short channel devices. Equation (3) gives the subthreshold current for short channel devices [4].

$$I_{Sub} = I_0 \left[1 - \exp\left(-\frac{V_{ds}}{V_t}\right) \right] \cdot \exp\left(\frac{V_{gs} - V_{th} - V_{off}}{nV_T}\right) \quad (3)$$

where,

$$I_0 = \mu \frac{W}{L} \sqrt{\frac{q \epsilon_s N_D}{2 \phi_s}} \cdot V_T^2 \quad (4)$$

$$V_{off}' = V_{OFF} + V_{OFFL} / L_{eff} \quad (5)$$

where,

n = Sub threshold slope factor ($1 < n < 3$)

I_0 = Process dependent parameter and also depends on device geometry

W/L = is the width to length ratio of MOS device

V_{gs} = Gate to Source voltage

V_T = Thermal Voltage, equal to $k_B T / q$,

Short channel effect is the variation of threshold voltage with respect to the channel length. The impact of SCE can be summarized as Sub threshold current, Drain Induced Barrier Lowering (DIBL), Gate Induced Drain lowering (GIDL), Channel length modulation (CLM) and velocity saturation. In a MOSFET device channel current is dependent on the gate voltage and the drain voltage. Thus the transistor modeling and the behavior can be well understood by I-V characterisation.

A. Sub-Threshold Leakage Current

Sub-threshold current, I_{sub} is the channel current which occurs when $V_{gs} < V_{th}$ i.e. for gate voltage lesser than threshold voltage of a transistor. This is the main cause for leaky transistors and static power dissipation in short channel devices. It has been investigated that for 180nm N-channel

device, drain current exists for even V_{gs} below 0 Volts as shown in Fig. 2. Though threshold voltage of transistor is $V_{th} = 530$ mV, “OFF” state leakage current of 20pA exist even for gate voltage of 0 volts as shown in table I. The range of threshold current is found to be 20pA to 16 μ A. This accounts for high leakage current in the device and leads to major static power consumption. This current can add up in complex CMOS circuits posing a design challenge for low power circuit design.

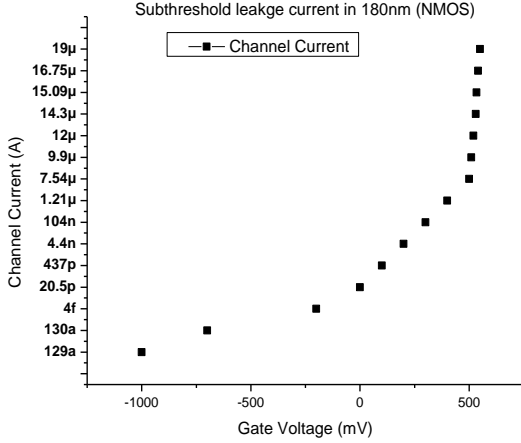


Fig. 2. Threshold voltage curve for 180nm nMOS Device

In case of 180nm transistor, I_{ds} increases exponentially and the curve resembles any other silicon transistor as shown in Fig. 2. The comparison between sub threshold current for 180nm transistor and 45nm transistor has been done in Fig. 3. It can be observed that leakage and “OFF” state current is more for 45nm transistor compared to 180nm. These figures show that sub threshold voltage curve is more linear in case of 180nm compared to 45 nm device. It has been investigated that that I_{sub} increases linearly for 180nm device, but follows a “U” curve for 45 nm device as shown below.

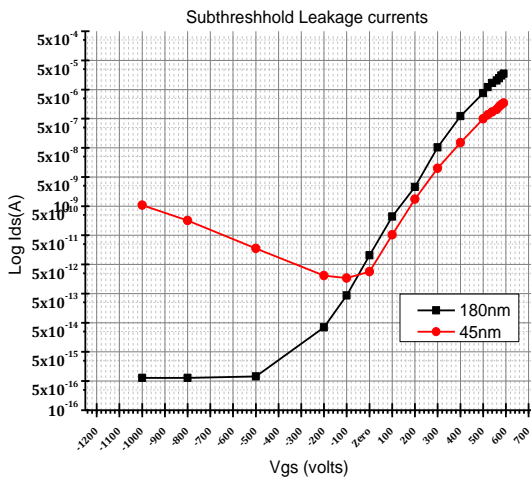


Fig. 3. Sub-Threshold current for 180 nm and 45 nm nMOS device

B. “OFF” State Leakage Current

Table I gives the readings taken from simulation carried out for both devices. The readings have been taken both for 180nm and 45nm technology nodes for V_{gs} ranging from

negative 1000mV to +590 mV at $V_{DS} = 2V$. Fig.4 shows the plot of simulation result of 45nm device for V_{gs} Vs. I_{ds} , below threshold region. The points M0, M, M2 and M3 give the trace of various points on the plot. Point M1 is measured at -1.96 with drain current as high as $1.61 \mu A$. This indicates presence of large “OFF” state leakage current in case of 45nm device compared to 180nm. This current is almost equal to drain current when the device is in saturation region. As 45nm process technology is the most advanced technology node today, with best available techniques applied at process level, it is required to mitigate these leakage currents at circuit level. This has been achieved by circuit designers at circuit level by keeping device cut-off from the ground by inserting switches, power-gating techniques and sleep transistor between circuit and power/ground rails.

TABLE I: SUBTHRESHOLD REGION CURRENT IN 180NM AND 45 NM NMOS DEVICE

V_{gs} (mV)	I_d (A) for 180nm	I_d (A) for 45 nm
-1000	129E-17	1.082E-9
-800	129E-17	324E-12
-500	143E-17	35.2E-12
-200	70E-15	4.13E-12
-100	86E-15	3.42E-12
0	20.5E-12	5.66E-12
100	437E-12	104E-12
200	4.55E-9	1.74E-9
300	1.04E-9	19.74E-9
400	1.218E-6	150E-9
500	7.54E-6	985E-9
520	12E-6	1.35E-6
540	16.7E-6	1.7E-6
560	20.5E-6	2.07E-6
570	24.6E-6	2.55E-6
580	30.1E-6	3E-6
590	35E-6	3.4E-6

Though leakage current is more for 45nm device in below zero volts, there exists more leakage current for 180nm transistor in the sub-threshold region. This improvement in 45nm device has been achieved by change in process material for fabrication of gate which reduces gate leakage current at high V_{DS} by reducing depletion width under drain.

An interesting behavior is observed in case of 45 nm N-channel MOSFET in Fig. 4. The characteristic curve with V_{gs} Vs. I_{ds} shows the plot of behavior of 45nm device below threshold voltage that is -2V to 560mV. The graph shows a U curve showing more leakage at negative and zero voltage, then increases slowly and turns around 240mV. It is proposed that, this high leakage region can be considered for ultra low power circuit designing with low input signals. But to avoid leakages threshold voltage has been increased to about 570mV by using different gate process technology. This limits ultra low power applications as transistor works in saturation region only above 600mV. Thus, this leakage current of 45nm device still remains a great challenge for circuit designers for low power applications.

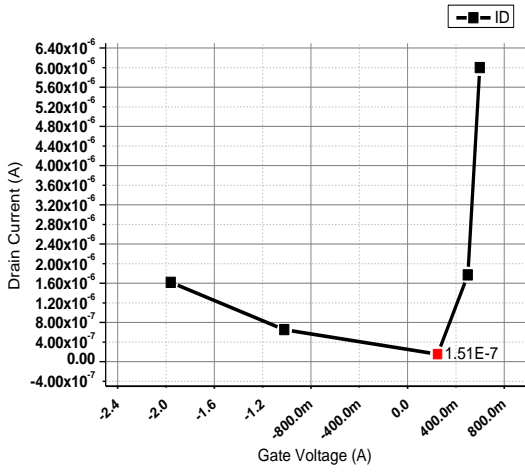


Fig. 4. U curve for 45nm transistor in subthreshold region.

As seen from above figure, there exist higher leakage current below zero volts than between 0- V_{th} volts (about 580mV)

IV. THRESHOLD VOLTAGE MODELING

MOSFETs have both process dependent and design dependent parameters. Threshold Variation is the process dependent parameter and plays an important role in CMOS circuit design. Threshold voltage is a process dependent parameter and remains constant for long channel devices i.e. for $L \geq 1\mu m$. But as discussed above, short channel devices show V_{th} variation due to short channel effects. In short channel devices, V_{th} also depend on the device parameters like channel length, channel width and drain voltage.

A. Threshold Voltage Equation for Long Channel Devices

The Threshold Voltage, V_{TO} , is defined as the gate potential V_G at which the surface potential Φ_s changes by $2\Phi_F$, i.e. the surface becomes strongly inverted [5].

$$V_{TO} = \left[\phi_{GC} - \frac{qN_{OX}}{C_{OX}} \right] + \left[-2\phi_F - \frac{Q_{BO}}{C_{OX}} \right] + \frac{qN_1}{C_{OX}} \quad (6)$$

where,

- ϕ_{GC} \Rightarrow the work function difference between gate and the channel.
- qN_{OX} \Rightarrow Positive charge density at the gate Si-oxide interface due to impurities and lattice imperfections at the interface (+ve sign)
- ϕ_F \Rightarrow the substrate Fermi potential
- Q_{BO} \Rightarrow Depletion charge density at surface inversion
- qN_i \Rightarrow Additional channel implant density (Sign is positive for p-type and negative for n-type implant)

$$\text{nMOS transistor: } Q_{BO} = -\sqrt{2qN_A\epsilon_{Si}}|-2\phi_F| \quad (7)$$

$$\text{pMOS transistor } Q_{BO} = \sqrt{2qN_A\epsilon_{Si}}|-2\phi_F|$$

$$\phi_{GC} = \phi_F - \phi_{F(gate)}$$

$$\phi_{F(gate)} = \begin{cases} 0.55V - N \text{ type polysilicon gate} \\ -0.55V - p \text{ type polysilicon gate} \\ \phi_M - \text{metal gate} \end{cases}$$

$$\epsilon_{OX} = 0.34 \times 10^{-12} \text{ Fcm}^{-1}, \epsilon_{Si} = 1.06 \times 10^{-12} \text{ Fcm}^{-1}, C_{OX} = \frac{\epsilon_{OX}}{t_{OX}}$$

$$Q_B = -\sqrt{2qN_A\epsilon_{Si}}|-2\phi_F + V_{SB}| \quad (8)$$

$$\begin{aligned} V_T &= \phi_{GC} - 2\phi_F - \frac{Q_B}{C_{OX}} - \frac{Q_{OX}}{C_{OX}} \\ &= \phi_{GC} - 2\phi_F - \frac{Q_{BO}}{C_{OX}} - \frac{Q_{OX}}{C_{OX}} - \frac{Q_B - Q_{BO}}{C_{OX}} \\ &= V_{TO} - \frac{Q_B - Q_{BO}}{C_{OX}} \end{aligned} \quad (9)$$

Using (8) and (9) we get, equation for threshold voltage with body bias effect and is given by (10)

$$V_{th} = V_{TO} + \gamma \left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|} \right) \quad (10)$$

where γ = body effect coefficient = $\frac{\sqrt{2qN_A\epsilon_{Si}}}{C_{OX}}$

Equation (10) is the most familiar threshold equation used for MOSFETs but this has been modeled considering long channel with uniform doping. Thus we see that, the threshold voltage in general depends upon seven factors and they are gate conductor material, gate Oxide material and thickness, substrate doping, Channel Ion Implantation (depending on the dopants type i.e. impurity added p-type (n-type), V_{th} is made more positive or negative, impurities in Silicon-oxide interface, Q_{OX} , source bulk voltage or body bias effect, V_{SB} and temperature, T . For $V_{SB} \neq 0$, threshold voltage is denoted as V_{th} .

B. Threshold Voltage for Short Channel Devices

Equation (11) has been used for derivation and modeling of threshold voltage of short channel devices [4].

$$V_{th} = V_{TO} + \gamma \left(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|} \right) \quad (11)$$

$$V_{TO(SCE)} = V_{TO} + \Delta V_{TO} \quad (12)$$

Here, V_{TO} represents long-channel threshold voltage at $V_{SB}=0V$ (typical value is 0.7V for NMOS and -0.7V for PMOS) Here, ΔV_{TO} represents a new process variation parameter added to V_{TO} .

$$V_{th(SCE)} = V_{TO(SCE)} + K1.(\sqrt{\phi_F - V_{SB}} - \sqrt{\phi_s}) - K2.V_{DS} \quad (13)$$

where $K1$, $K2$ and V_{TO} are implemented as model parameters for model flexibility. For short channel devices, threshold voltage is also dependent on non-uniform lateral doping, short channel effects causing dependence on channel length and channel width, and drain supply voltage due to DIBL effect. The variation of threshold voltage with respect to SCE and DIBL is modeled as given in (14):

$$\Delta V_{th}(SCE, DIBL) = -\theta_{th}(L_{eff}).[2(V_{bi} - \phi_F) + V_{ds}] \quad (14)$$

where,

V_{bi} is known as the built in voltage of the source/drain junctions and is as given below:

$$V_{bi} = \frac{k_B T}{q} \ln \left(\frac{N_{DEP} N_{SD}}{n_i^2} \right) \quad (15)$$

Here, N_{SD} is doping concentration of source/drain diffusion. Thus, it can be concluded that deep-sub-micron levels devices show process and design parameter variations called as parameter variability due to non-uniform doping, variations in channel length and drain voltage.

C. Variation of V_{th} with Respect to Length

Threshold voltage is very important design parameter for any transistor. Since transistors at deep submicron levels show a great variation in V_{th} due to various factors like DIBL and other short channel effects, it has been the most focused design issue. We see that the SCE are more prominent in short channel devices where silicon di-oxide is used as gate material. Also, threshold voltage is found to be varying with respect to various parameters such as supply voltage V_{DS} , channel length L , channel width W and temperature. Table II shows dependence of threshold voltage on channel length for 180 nm devices. The threshold voltage along the channel is modified due to the non-uniform substrate charge and is explained by charge channel model in [4].

TABLE II: THRESHOLD DEPENDENCE ON CHANNEL LENGTH IN 180NM

SL	Channel width=2 μ , temp=27°C		
	Channel length(nm)	V_{th} (mV)	Leakage power (W)
1	180	0.527	2.51E-3
2	360	0.488	1.677E-3
3	540	0.481	1.145E-3

For 180nm technology node we observe that threshold voltage decreases with increasing L leading to more leakage currents in circuits. To design CMOS circuits in order to achieve gain, proper rise time and fall time, bandwidth and high speed operations it is required to size aspect ratio of both NMOS and PMOS. Dependence of V_{th} on channel length and width can cause dynamic V_{th} variations causing unpredictable behavior of circuits. The dependency of threshold voltage on L and W has been explored in circuit designs in [6]. This dependency of threshold voltage and leakage current on aspect ratio is technology and process dependent.

D. Drain Induce Barrier Lowering-DIBL

DIBL effect is the reduction of threshold voltage due to the influence of drain voltage. This effect becomes more prominent as channel length decreases. This effect of DIBL has been well corrected in 45nm technology node by replacing the process material polysilicon by high- k dielectric material. Fig. 5 shows transfer characteristics for different drain voltages and it can be observed that threshold voltage reduces as V_{DS} is increased (towards left) between 1-5 volts. Taur & Ning has come out with this observation in [7], which states that as high drain voltage is applied to a short channel device; the barrier is lowered resulting in further decrease of the threshold voltage.

The maximum threshold voltage for 180nm technology is 540 mV (point M5), for $V_{DS} = 1V$. The least threshold voltage value in graph is 326mV for $V_{DS} = 5V$ shown by point M1. These simulations have been carried out room temperature for constant gate voltage, $V_{gs} = 1.8V$. The simulations have

been carried out using transistor size $W/L=2\mu/180nm$. The variation of V_{th} , with respect to the drain voltage V_{DS} is caused due to the extension of depletion width below drain region and thus influence of free charge carriers by high drain voltage.

This leads to the formation of close channel between source and drain resulting in flow of more drain current. This impact of drain voltage is called as Drain Induces Barrier Lowering called as DIBL.

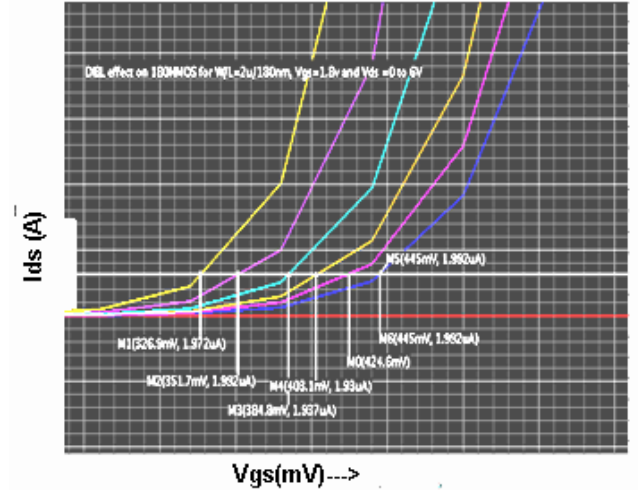


Fig. 5. DIBL effect on threshold voltage (180m).

As seen from Fig. 6, DIBL effect is more in case of 180 nm node compared to 45 nm. This has been improved by changing the process material between gate and channel. Table III shows the effect of DIBL for both 180m and 45nm nMOS transistors for range of drain voltage varying from 1V-5V.

TABLE III: VARIATION OF THREHSDOLD VOLTAGE DUE TO DIBL

Temp=27°C		
V_{DS} (V)	Threshold Voltage (180nm)	Threshold Voltage(45nm)
0.05	608mV	590mV
1	550mV	587mV
2	547mV	585mV
3	442mV	584mV
4	440mV	573mV
5	380mV	-

Modeling of short channel devices clearly show that threshold voltage in case of short channel devices depends on two factors apart from V_{th} as shown in (12) and is given by $V_{TO(SCE)} = V_{TO} + \Delta V_{TO}$. The second term, ΔV_{TO} , represents variability of threshold voltage with respect to short channel effects and Drain Induced barrier Lowering and has been given by (14). These variations in threshold voltage are caused due to change in channel length referred as effective channel length, built in bias voltage between source and drain terminals caused by the presence of lateral and vertical fields and high drain voltage. The doping concentration and process materials also play an important role for this variability. Thus as indicated by ITRS 2011, short channel devices have

exhausted innovations in process materials and these leakage and power issues may be further improved at design level and architecture level [8].

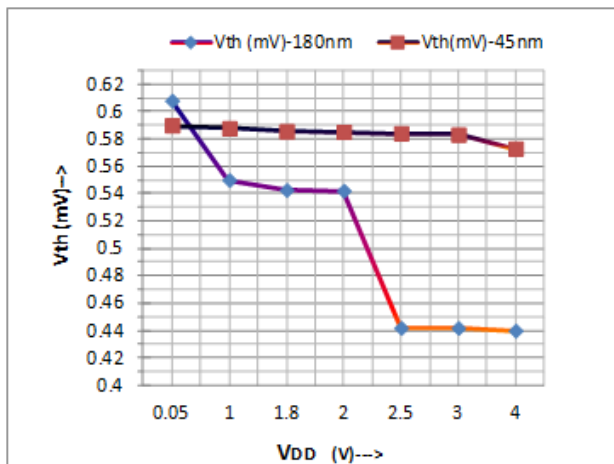


Fig. 6. Threshold variation with supply voltage-DIBL

Fig. 6 indicates improvement in DIBL effect in case of 45nm N-Channel MOSFET. This has been achieved by deviation from conventional polysilicon and silicon dioxide gate structures to innovations in process technology by using high-k dielectric material and metal gate with strain implementation techniques.

V. CONCLUSION

This paper presents the results of extensive simulations carried out for 180 nm and 45 nm nMOS transistors. This paper presents the results of study of impact of short channel effects and design parameter variations caused in deep submicron devices. The simulation results show that "OFF" state leakage current and subthreshold leakage current are the main source of power consumption in short channel devices.. Though DIBL effect and other short channel effects have been improved in 45nm devices by change in process material change of gate, "OFF" state leakage current is much higher compared to upper technology nodes. Also modeling of threshold voltage show that the process design parameter, threshold voltage, was constant in long channel devices. But at deep submicron levels it varies with respect to length, width and supply voltage causing major challenge for CMOS circuit designers. These variations can be mitigated improved at circuit and architecture levels using power gating, multi- V_{th} and multi- V_{DD} techniques.

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