

Enhanced Scan in Low Power Scan Testing

Sangeetha Upadhyayula, *Member, IACSIT*

Abstract—A routing-aware architecture is introduced to reduce capture power and peak test power. For shifting of test data or capturing the test responses, only a subset of scan-flip flops are activated in any clock cycle. This process can effectively reduce the capture power and peak test power. In order to reduce routing overhead, two routing driven architectures were proposed. Increase in performance levels were observed in making the proposed scan architecture, more automatic, by automatic shifting of register which requires less number of signals. Results were obtained by experimenting to this proposed scan architecture in reducing capture power, peak test power, test data volume and test application cost.

Index Terms—Power, capture power, peak test power, automatic shift register, test application cost and test data volume.

I. INTRODUCTION

For testing sequential circuits, in these modern trends, having large portion of logic, design for test (DFT), and implementing ‘scan test’ are mandatory parts of the design process.

This reduces the complexity of testing sequential circuits. The basic concept of a ‘Scan Test’ is to connect memory elements like flip flops or latches forming chains, so that shifting through scan chains allows to control and observe the states of circuit under test (CUT).

Many testing methods were proposed in order to test the sequential circuits to make the circuit fault-free. Those methods include capture power, peak test power, test data volume and test application cost. Various methods were proposed in order to reduce capture power and peak test power [1] - [4].

An ‘Enhanced Scan Forest’ [4] is introduced to reduce test power, test data volume, test application cost. Two routing driven schemes were proposed to reduce routing and area overhead problems.

Capture power: It is a special test power that is produced at capture cycles, which is proportional to the maximum transitions generated at the capture cycles.

Peak test power: It is usually proportional to the maximum transition produced at single clock cycle.

‘Scan forest’ was first proposed [5] to reduce test data volume and test application cost. In this architecture, almost all the scan flip flops are connected to ex-or trees. Area and Routing overheads were still there.

A ‘Reconfigured Scan Forest’ was presented [6] in which only leaf scan flip flops were connected to ex-or network. The output from this network is connected to test response

compaction. Comparatively in reconfigured scan forest, area and routing overhead are much less than ‘scan forest’.

After this, ‘Two-Stage Architecture’ was also presented [7]. This reduces average test power effectively. Based on two stage architecture, all the scan flip flops must be connected to ex-or trees. Here also, the area and routing overhead problems were arisen. Hence the above three scan architectures cannot effectively reduces peak test power and capture power.

Test application cost can be reduced by efficient test generation schemes [8]. Techniques were introduced for the reduction of test data volume and test application time [9] [10].

II. NEW MODIFIED ARCHITECTURE

Now, new scan architecture as shown in fig: 1, called ‘Modified Enhanced Scan Forest’. This is a modified version of enhanced scan forest and so the name called ‘Modified Enhanced Scan Forest’.

The enhancement in this new scan architecture is that, this architecture is more automatic than the original ‘Enhanced Scan Forest’ [4] in which the pins ‘X₁’ and ‘X₂’ are manually given. Due to this type of manual process, at every time, during the change of values of ‘X₁’ and ‘X₂’, errors may arise in assigning values to those pins. This is the major demerit of that original scan architecture.

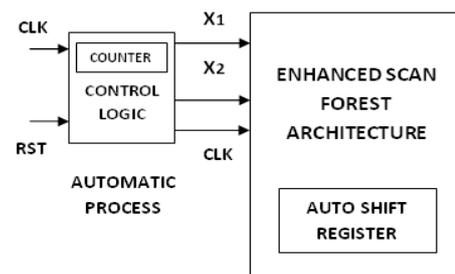


Fig. 1. Modified enhanced scan forest

In order to avoid it, we are going for automatic assigning of values to those pins by the usage of ‘Control Logic’ in the architecture. This is the modification the scan architecture. Hence it became more automatic due to the usage of ‘Control Logic’ in the scan architecture than before [4]. This is the major advantage of modified scan architecture. In this the errors which arise in original scan architecture [4] will be avoided.

The two stage partitioned scan architecture reduces capture power and peak test power. The first stage includes multiple scan chains and Second stage includes multiple scan trees which contain multiple scan chains. The outputs of the scan flip flops in the first stage are connected to scan flops in

the second stage which means that the scan trees in the second stage are driven by scan chains in the first stage.

The output of the scan trees is given to ‘Test Response Compactor’ which is used to compact the test responses. It may become the extra overhead. The number of scan outs from the compactor is based on our requirement.

The ‘Control Logic’ is programmed with the usage of a counter in it for making it as ‘automatic assigning of values’ through the counter. The clock is given to the control logic too as shown in the fig: 1. ‘Reset’ pin is also used in order to reschedule the count value by clearing the counter according to the program.

The functioning of control logic is as follows:

Step 1: Initialize $X_1 = 1$; $X_2 = 0$; count = 0; set the circuit in test mode.

Step 2: Run till count < N; N specifies the length of scan chain and scan length.

Step 3: If (count = N) $X_1 = \sim X_1$; $X_2 = \sim X_2$;

Step 4: Run till (count = N + N); N + N = runs for part to part stages i.e. subset of scan trees

Step 5: If (count = 2N), go to step: 1.

An automatic shift register is used to control the clock signal of all flip flops. Only one cell of the register is assigned the value ‘1’ which activates the flip flops from first stage to second stage subset by subset each time. Only the activated scan flip flops will capture test responses at capture cycles. Rest of the flip flops are disabled at that time.

By changing the register value from 100...00 to 010...00 and so on., all the subsets of scan flip flops in the second stage will be activated subset by subset until all the subsets of scan flip flops are activated. This period includes ‘(R-1) C_2 ’ clock cycles, where ‘R’ is the size of automatic shift register. Then the circuit is kept in functional mode.

As soon as the scan flip flops in the second stage are enabled, they will capture the test responses in capture cycles and the test responses are shifted out. Now, reload the test data placed in the first stage to the scan flip flops in the second stage in ‘ C_2 ’ clock cycles. At this moment the first stage is kept in functional mode.

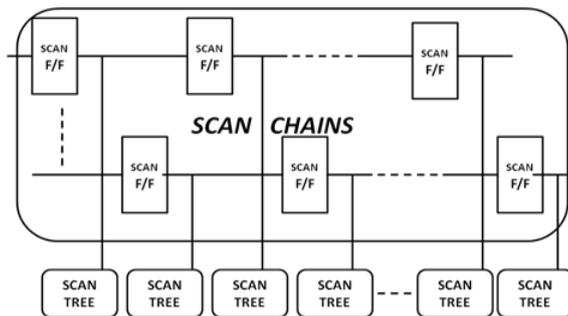


Fig. 2. Scan chain architecture

As the register value once again starts from the initial value, the clock signal is given to the first stage and the scan flip flops in the first stage will be activated and the second stage scan flip flops go to disabled mode.

At this stage, the test responses are captured from the first stage and the responses are shifted out in ‘ C_2 ’ clock cycles. This period includes ‘(R-1) $C_2 + R$ ’ cycles. The process will go on like this. Hence the number of clock cycles required

to apply all the test vectors to scan architecture based on the new scan architecture is,

$$C = (C_1 + 2 C_2 (R - 1) + R + 1) V + C_1$$

where C is number of clock cycles;

V is number of test vectors.

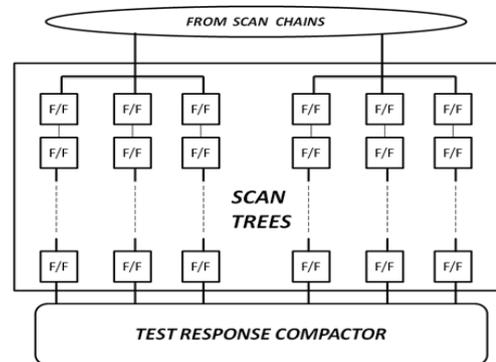


Fig. 3. Scan tree architecture

III. TWO ROUTING SCHEMES

A. After Grouping

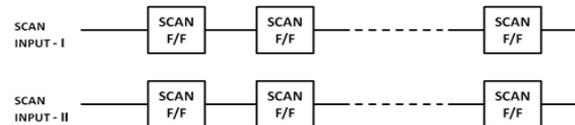


Fig. 4. Forming scan-chains with scan flip flops from each group from the nearest scan-in pin.

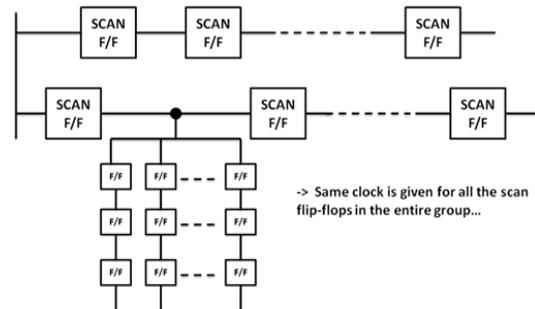


Fig. 5. Attaching the scan trees from nearest scan in pin

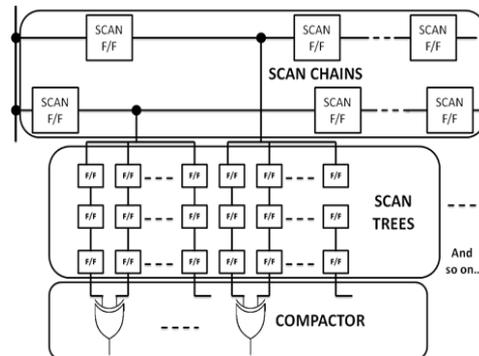


Fig. 6. Attaching all the subsets of scan-trees from the nearest scan-in pin till the entire scan chains outputs are connected to which ex-or trees are connected which is called as compactor.

B. Before Grouping

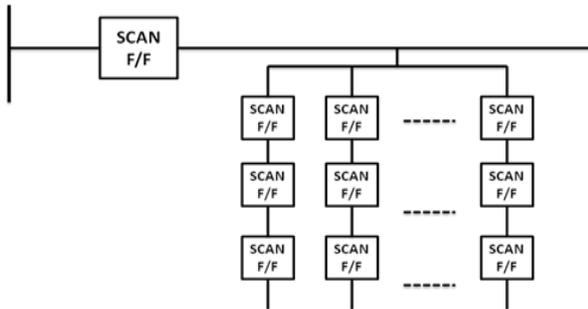


Fig. 7. Attaching a scan flip flop to nearest scan-in pin from group and attaching scan-chains which forms scan tree.

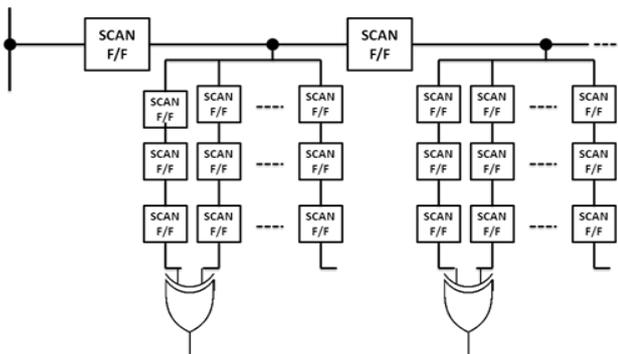


Fig. 8. Attaching another scan flip flop to initial one to which another scan tree is to be attached as shown above

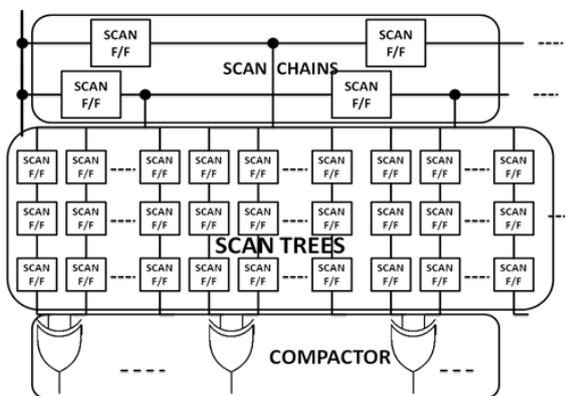


Fig. 9. Forming scan trees (having multiple scan chains) and attaching them to the outputs of entire scan chains to which ex-or trees are attached which is called as compactor

IV. EXPERIMENTAL RESULTS

The proposed method has been implemented in VHDL programming and run on a desktop computer. The proposed architecture produce much less peak test power and capture power for all circuits. The modified enhanced scan forest obtains very good results for test application time reduction ratio and test data compression ratio. An example was taken to implement this proposed modified enhanced scan architecture, which was a 16X1 multiplexer (designed with two 8X1 and with one 2X1 multiplexers). It is programmed

and was implemented as shown in fig. 10.

The performance levels of this proposed modified enhanced scan architecture has increased as it became ‘more automatic’ with the usage of ‘automatic shift register’ which requires less number of signals for its operation. As it is more automatic the time taken for operation became less and the time consumption has reduced for its application and process.

V. CONCLUSION

Modified enhanced scan architecture is proposed for increase in performance levels through the usage of automatic shift register. This architecture is made more automatic, than before, with the usage of control logic. Experimental results shows that the proposed modified architecture with automatic process reduces the number of clock cycles required for operation which indicates the reduction of test power and less number of test vectors are sufficient to test this architecture. Routing overhead of this architecture can be reduced with proposed two routing-driven schemes.

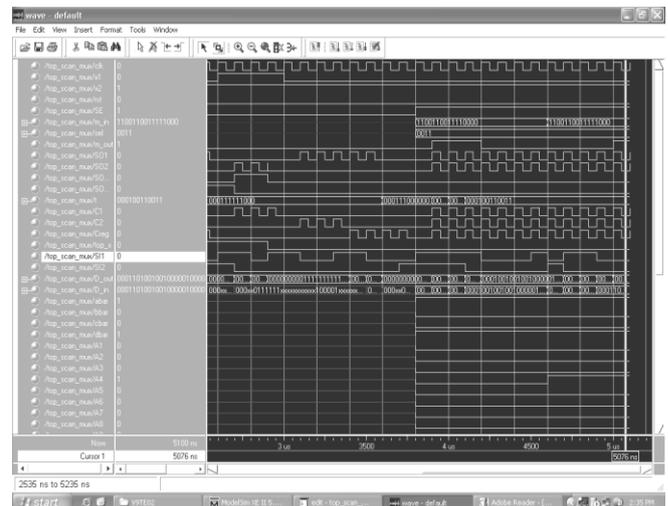


Fig. 10. Snapshot of 16x1 multiplexer (using two 8x1 and one 2x1 multiplexers) which is implemented based on this proposed modified enhanced scan architecture

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S. Upadhyayula was born at Tenali, (Guntur District, Andhra Pradesh, India) on 20th April 1987 and the Educational qualifications include, Masters in Technology, with the specialization, Digital Systems and Computer Electronics in Jawaharlal Nehru Technological University, Ananthapur, Andhra Pradesh, India in the year 2012 and Bachelors of Technology with the specialization, Electronics and Communication Engineering in Siddharth Institute of Engineering and Technology, K., Puttur, Chittoor District, Andhra Pradesh, India in the year 2008.

Currently she is working as an ASSISTANT PROFESSOR (Electronics and Communications Department) in Turbomachinery Institute of Technology and Sciences, Patancheru, Hyderabad, Andhra Pradesh, India from a year. Her interested Research areas include Very Large Scale Integration (VLSI) Design.

Mrs. Upadhyayula is a member in IACSIT (International Association of Computer Science and Information Technology).