A New Low Power Single Bit Full Adder Design with 14 Transistors using Novel 3 Transistors XOR Gate

Manoj Kumar, Sandeep K. Arya, and Sujata Pandey

***Abstract*—In present work a new XOR gate using three transistors has been proposed. Design shows adequate output logic levels with noise margin of 2V with 3.3V input signals. XNOR logic, obtained with addition of inverter shows improved noise margin of 3.2V. A new design for single bit full adder has been implemented using proposed XOR/XNOR gates and transmission gate multiplexer. Full adder designed with 14 transistors shows power dissipation of 655.6149μW and maximum output delay 0.11055ns. Proposed adder circuit shows adequate noise margin of 3.2 V for Sum (Sum output) and 2.2V for Cout (Carry output) with supply voltage of 3.3V. Circuit works well with reduced supply voltage and simulations have been carried out up to 1.8V supply voltage. Simulations are performed by using SPICE based on TSMC 0.35μm CMOS technology. Power consumption of proposed full adders has been compared with earlier reported circuits and proposed circuit's shows better performance in terms of power consumptions and transistor count.**

***Index Terms*—CMOS, exclusive-OR (XOR), exclusive-NOR (XNOR), full adder design, low power and transmission gate.**

I. Introduction

Research efforts in the field of low power VLSI (very large-scale integration) systems have increased many folds due to exponential growth of portable electronic devices like laptops; audio/video based multimedia and cellular communication devices. With rise in number of transistors on chip, power consumption of VLSI systems is also raising which further, adds to run time failures and reliability problems. Packaging and cooling mechanism become more complex and costly with excessive power consumption. Low power consumption is one of important design criteria for IC designers at all levels of design along with delay and area considerations. Faithful functionality of device at lowest supply voltage is also vital consideration.

Three major source of power consumption exists in CMOS VLSI circuits: 1) switching power due to charging and discharging of node capacitances, 2) short circuit power due to short current flow from power supply to ground with simultaneous functioning of p-network and n-networks, 3) Static power consumption due to leakage currents.

Power consumption of VLSI circuits can be reduced by scaling supply voltage and capacitance. With the reduction in supply voltage, problems of small voltage swing, insufficient noise margin and leakage current starts to instigate.

Addition of two binary numbers is fundamental and most frequently used arithmetic operation in microprocessors, digital signal processors (DSP), and application-specific integrated circuits (ASIC) etc. Single bit binary adders are significant building blocks in VLSI circuits and efficient implementation of these adders will affects the performance of entire system. In recent years different types of adder using various logic styles have been proposed in literature. Standard CMOS 28 transistor adder using pull up and pull-down networks having equal number of NMOS and PMOS transistors is reported in [1]. Complementary pass-transistor logic (CPL) with 32 transistors having better driving capability with high power consumption is reported in [2].Transmission gate CMOS adder (TGA) based on transmission gates with 20 transistors is reported in [3]. Main disadvantage of TGA is that it requires double number of transistors than pass transistor logic for implementations same logic function. A transmission function full adder (TFA) is based on transmission function theory and used 16 transistors [4]. Multiplexer based adder (MBA) using 12 transistors with elimination of direct path to power supply reported in [5]. Static energy recovery full (SERF) adder with 10 transistors with reduced power consumption at the cost of large delay is presented in [6]. Another design with 10 transistors full adder by using XOR/XNOR gates also reported in [7]. A hybrid CMOS logic style adder with 22 transistors is reported [8]. In [9] a full adder using 22 transistors based on hybrid pass logic (HPSC) is presented. Full adder for embedded applications using three inputs XOR is reported in [10]. In [11] a 16 transistor full adder cell with XOR/XNOR, pass transistors and transmission gate is reported. The function of full adder is based on following two equations, *A*, *B*, C_{in} are the three single bit inputs and generates two outputs of single bit Sum and C_{out}, where:

$$Sum = (A \oplus B) \oplus C_{in} \tag{1}$$

$$C_{out} = A.B + C_{in}(A \oplus B) \tag{2}$$

Structured approach for implementation of single bit full adders [12] using XOR/XNOR is shown in Fig. 1. With decomposition of full adder cell into smaller cells, equations (1) and equations (2) can be rewritten as

$$Sum = H' xnor C_{in} = H.C_{in}' + H'C_{in} \tag{3}$$

$$C_{out} = AH' + C_{in}H \tag{4}$$

where H is half sum $(A xor B)$ and H' is complement of H.

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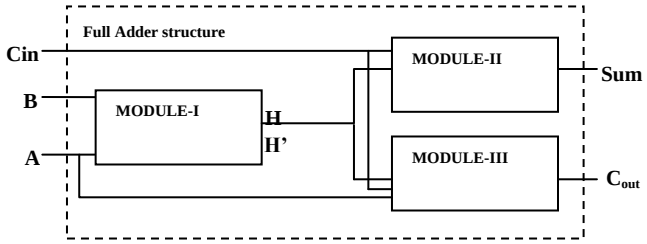


Fig. 1. Structure of single bit full adder

A large number of reported full adder circuits have been implemented with XOR/XNOR gates and performance of these XOR/XNOR gate also affects the performance of adder circuits. The exclusive–OR (XOR) and exclusive–NOR (XNOR) gates are the basic building blocks of full adder circuits. The XOR/XNOR gate can be implemented using AND, OR, and NOT gates but shows high redundancy [1]. Optimized designs of these gates will certainly improve the performance of VLSI systems as these gates are used as sub block in larger arithmetic circuits. XNOR/XOR designs with reduced number of transistors having adequate performance levels are extremely useful for efficient implementation of the large system such as adders, multipliers etc. XOR gates based on eight transistors and six transistors have been used in [1], [13]. Four transistors pass transistor based XOR gates with limitation of driving capability are reported in [14]. Various designs for XOR and XNOR gates using four transistors also presented in [7], [15], and [16]. Three inputs XOR design in place of two inputs is reported in [17]. XOR/XNOR design with ten transistors based on transmission gates is reported in [18]. XOR/XNOR circuits with dual feedback also reported in [19], [20].

At circuit level, an optimized design is necessary with reduced numbers of transistors, less power consumption and with adequate output voltage level. Here, in current work a new XOR gate with three transistors has been proposed. A new single bit full adder with 14 transistors based on proposed XOR gate and transmission gate multiplexer has been presented. The rest of paper is organized as follows: In Section II, a new 3 transistor XOR gate has been reported. Further, XOR/XNOR cell and a single bit full adder have been designed. In section III results of proposed single bit full adder designed in previous section have been presented and compared with earlier reported circuits. Section IV concludes the work.

II. System Description

Proposed design for XOR with three transistors has been shown in Fig. 2. In proposed XOR, gate lengths of all three transistors have been taken as 0.35 μm. Widths (W_n) of NMOS transistor (N1) has been taken 0.5 μm. Width (W_p) for PMOS transistors (P1 & P2) have been taken as 4 μm. In proposed circuit when A=B=0 output is low because P1 and P2 transistor are on and logic 0 is passed to output. With input combination of A=0 and B=1 circuit show high output as transistor P2 is on while transistors N1 & P1 are off and high logic is passed to output node. In another case when A=1 and B=0, transistor P1 is on and high logic is passed to output node. In this case with A=1 transistor N1 also turns on and starts discharging the output node but the resistance of N1 has been made high by reducing its width. For acceptable output logic level for certain input combinations (W/L) ratios have been sized. Width of P1 and P2 has made large to reduce resistance while width of N1 is reduced for slow discharging. The voltage degradation due to threshold drop can be reduced by increasing W/L ratio of transistor of N1. The following equation [21] relates the threshold voltage with gate length and width of MOS transistor.

$$V_T = V_{T0} + \gamma\left(\sqrt{V_{SB}+\phi_0}\right) - \alpha_l \frac{t_{ox}}{L}\left(V_{SB}+\phi_0\right) - \alpha_v \frac{t_{ox}}{L} V_{ds} + \alpha_w \frac{t_{ox}}{W}\left(V_{SB}+\phi_0\right) \quad \text{---(5)}$$

where V_{t0} is the zero bias threshold voltage, γ is bulk threshold coefficient, ϕ_0 is 2 ϕ_F and ϕ_F is Fermi potential, t_{ox} is the thickness of oxide and α_l, α_v and α_w are the process dependent parameters. From (5) it is apparent that by increasing the W it is possible to reduce the voltage degradation. In last case when A=B=1, output node show low logic as transistor N1 is on, so proposed circuit works as XOR gate.

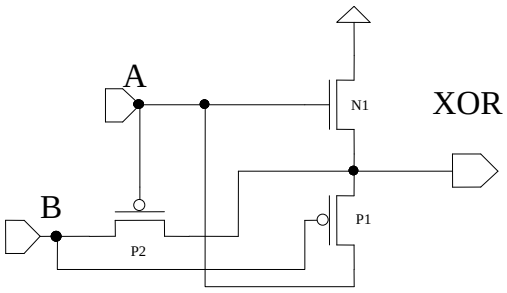


Fig. 2. Design of proposed 3 transistor XOR gate

XNOR operation has been obtained with addition of inverter. Complete XNOR/XOR module with five transistors has been shown in Fig. 3 Width for P3 (W_p) and N2 (W_n) have been taken as 2.5 μm and 1.0 μm respectively.

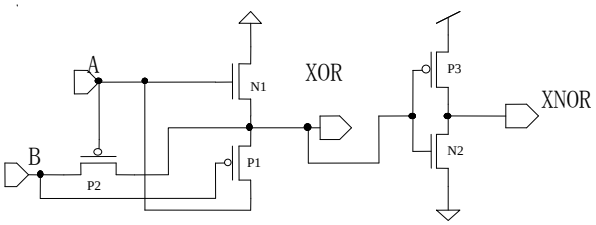
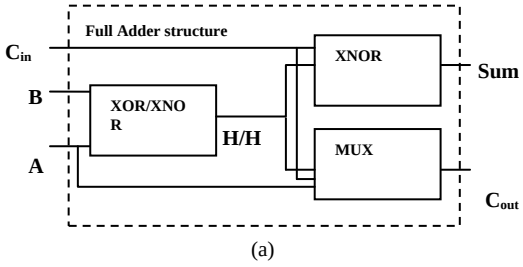


Fig. 3. Design of proposed XNOR/XOR cell

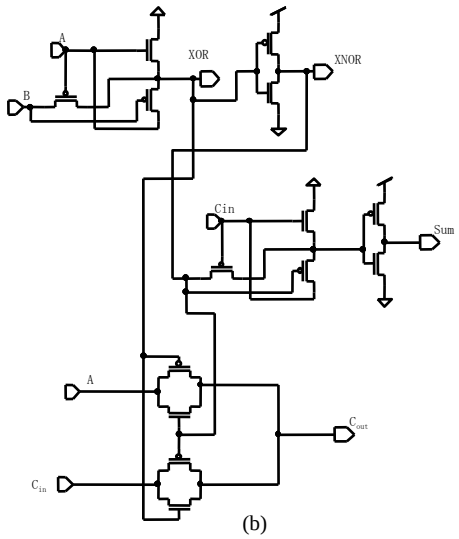
The full adder circuit can be implemented by various combinations of XOR/XNOR gates and multiplexer blocks. In present approach as shown in block diagram of Fig. 4 (a), we have used two XOR/XNOR cells and transmission gate multiplexer with four transistors to design the full adder.

Sum is generated by two XNOR gates as in equation (3) and Cout is generated by four transistor transmission gate multiplexer MUX as in equation (4). Two transistor multiplexers based on pass transistor logic can also be used to generate Cout which reduces the total transistor count of adder to 12. Since pass transistor logic shows poor noise margin so in current design transmission gate multiplexer approach has been utilized. For transmission gate multiplexer complementary gate control signals are required and in

current design both XOR and XNOR signals are already generated. The single bit full adder using proposed XOR/XNOR cell using 14 transistors has been implemented and shown in Fig. 4 (b). For multiplexer section values of width (Wn & WP) for NMOS and PMOS transistors have been taken as 1.0 µm & 2.5 µm respectively. Simulations also have been carried out with varying supply voltage from [3.3-1.8] V.



(a)



(b)

Fig. 4. Full adder using XOR/ XNOR gates and multiplexer (a) Block (b) Schematic diagram

III. Results and Discussions

Simulations have been performed using SPICE based on TSMC 0.35 µm CMOS technology with supply voltage of 3.3V. Fig. 5 shows the input and output waveform results for proposed XOR and XNOR gate. Table-I shows minimum voltage level of high and maximum voltage level of low output signals for XOR and XNOR gate. Proposed XOR gate provide sufficient output voltage level and noise margin of approximately 2V with 3.3V input signals. Output voltage levels are improved with addition of inverter in XNOR gate with noise margin of approximately 3.2V and design show full swing operation.

Table II shows power consumption, output delay, output voltage levels for sum and carry of proposed 14 transistors (14T) adder. Proposed adder show power consumption of 655.6149 µW with maximum output delay of 0.11055ns. Noise margin of 3.2 V and 2.2V have been obtained for Sum and C_{out} respectively with 3.3V power supply. Fig. 6 shows the input and output waveform results for proposed full adder circuit. Simulations also have been carried out with varying supply voltage to show its effects on power consumption & delay as shown in Table II. Fig. 7 show that power consumption varies from [655.614-132.003] µW with variation in supply voltage from [3.3-1.8] V. Fig. 8 show that delay varies from [0.11055-0.1655270] ns with variation in supply voltage from [3.3-1.8] V. It has been observed from Fig. 7 and Fig. 8 that power consumption reduces whereas delay increase with reduction in supply voltage..

Adders reported in [3], [4], [8], [9], [11] have been simulated and comparison have been presented in Table-III. It has been shown that proposed adder show less power consumption as compared to TGA 20T [4], 22T HPSC [9] and 22T hybrid [8] adder with less number of transistors. Proposed circuit also show superiority in terms of transistor count as compared to 16T [11], 18T [3] adder with minor concession in power consumption.

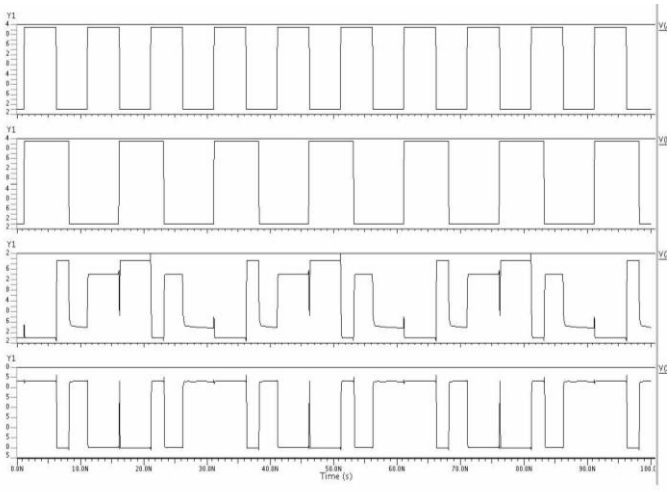


Fig. 5. Input and out waveform for XOR/XNOR gates

TABLE I: Output Levels Variations with Supply Voltage for Proposed Xor and Xnor Gate

Supply voltage (V)	Minimum level for high XOR output (V)	Maximum level for low XOR output (V)	Minimum level for high XNOR output (V)	Maximum level for low XNOR output (V)
3.3	2.402	0.42	3.29	0.025
3.0	2.179	0.42	2.99	0.1193
2.7	1.95	0.40	2.69	0.00419
2.4	1.72	0.40	2.39	000119
2.1	1.488	0.40	2.09	0.00032
1.8	1.24	0.40	1.79	0.00011

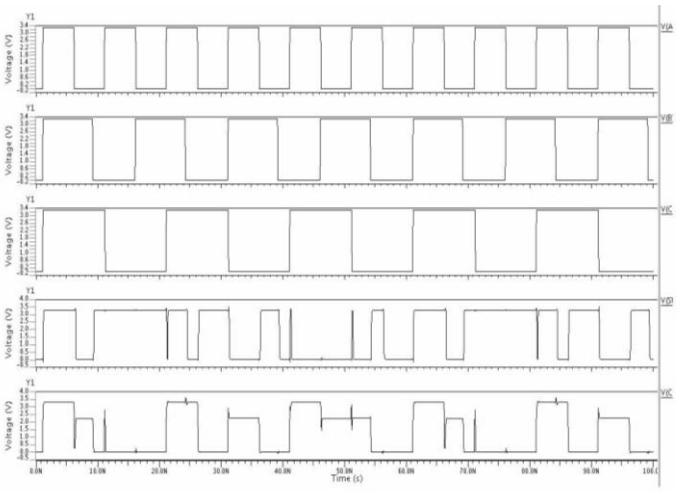


Fig. 6. Input and out waveform for proposed 14 transistor adder

TABLE II: POWER CONSUMPTION, DELAY AND OUTPUT LEVELS VARIATIONS WITH SUPPLY VOLTAGE FOR PROPOSED FULL ADDER

Supply voltage (V)	3.3	3.0	2.7	2.4	2.1	1.8
Power consumption (μW)	655.61	515.33	395.68	293.28	205.75	132.003
Maximum output delay (ns)	0.11	0.11	0.12	0.13	0.14	0.16
Minimum level for high sum (V)	3.29	2.99	2.69	2.39	2.09	1.79
Maximum level for low sum (V)	0.019	0.016	0.007	0.0026	0.0011	0.0009
Minimum level for high Cout (V)	2.21	1.98	1.74	1.50	1.25	1.01
Maximum level for low Cout (V)	0.0249	0.012	0.004	0.001	0.0005	0.0004

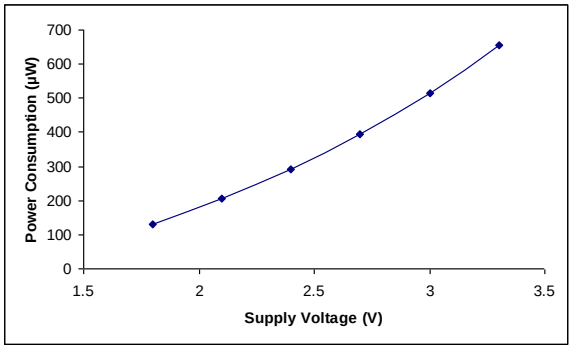


Fig. 7. Power consumption of adder with supply voltage

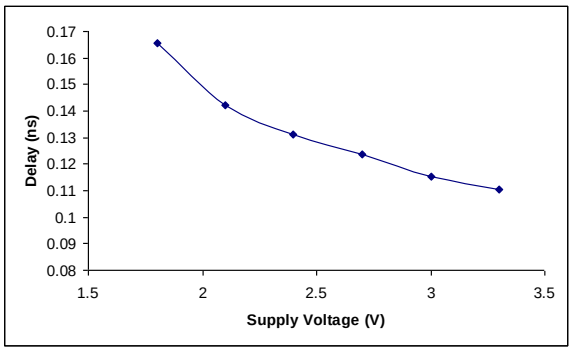


Fig. 8. Delay of adder gate with supply voltage

TABLE III: COMPARISONS OF PROPOSED FULL ADDER WITH EARLIER CIRCUITS

Adder configuration	Power consumption (μW)	Number of transistors for design
TGA20T [4]	1255.54	20
16T adder [11]	591.07	16
22T HPSC adder [9]	1533.9	22
18T [3]	617.23	18
22T hybrid adder [8]	1836.4	22
14T [present work]	655.614	14

IV. CONCLUSIONS

In reported work a new design for XOR gate with three transistors is proposed and single bit full adder based on XOR/XNOR gates using 14 transistors has been designed. Proposed adder shows power consumption of 655.614μW and maximum output delay of 0.11055ns with supply voltage of 3.3V. Simulation results show that proposed adder works properly with reduced supply voltage up to 1.8 V and show power dissipation of 132.003μW with maximum delay of 0.1655270ns. Proposed adder also show adequate noise margin with reduced supply voltage. Adder has been compared with earlier reported circuits and show less power consumption with reduced transistor count than earlier reported circuits.

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