A New Low Voltage Low Power Fully Differential Current Buffer and Its Application as a Voltage Amplifier

L. Safari and S. J. Azhari

***Abstract*—In this paper a novel low voltage low power fully differential current buffer with high CMRR is introduced. The proposed current buffer is designed and simulated with HSPICE in TSMC 0.18µm CMOS process and supply voltage of ±0.75V. The simulation results show 39.5Ω and 5.64KΩ differential mode and common mode input resistances respectively. The differential mode input impedance is 142.7 times smaller than the common mode one which is a unique feature. This result is quite significant when it is considered that in the conventional current buffers differential mode input resistance is equal to common mode one. The proposed current buffer exhibits a CMRR of 72.2dB and consumes only 83.9µW. PSRR+ and PSRR- are 160dB and 120dB respectively which make the proposed current buffer very suitable for mixed mode designs. Application of the proposed current buffer as a voltage amplifier is also presented which benefits from the outstanding property of independency of gain from related -3dB bandwidth.**

***Index Terms*—Current mode, low input impedance stage, fully differential current buffer, gain bandwidth independency.**

I. Introduction

Compared to voltage-mode circuits current-mode ones have such advantages as high slew rate, high bandwidth, simple circuitry and low voltage operation [1],[2]. Due to the small voltage swings associated with the low-impedance nodes, current-mode circuits can operate with low power supply voltages. Low voltage operation of current mode circuits has gained more importance due to today's semiconductor technology scaling down trend and reliability issues. This trend of technology has led to the popularity of mixed-mode System-on-Chips (SOCs) in which analog and digital circuits are integrated on one chip. Thus along with low voltage operation, analog designers have to concern about power supplies and ground fluctuations caused by the switching of the digital portion of mixed analog-digital circuits. Hence low voltage structures with PSRR and CMRR so high to suppress those noticed noises as well as other unwanted common mode signals are critically needed. Fully differential signal processing is commonly used in many fields mainly because of its inherent immunity to common mode signals, clock feed through, interferences and other types of common mode disturbances [3].

Current buffers are one of the main building blocks of current mode signal processors. They are widely used in current mode signal processing independently [4],[5] or as input stage of those circuits [6],[7]. Current buffers can also be used in voltage amplifier configuration as shown in Fig.1 providing interesting property of independent voltage gain and bandwidth [8]. Unlike voltage operational amplifiers which exhibit a narrow bandwidth that is highly dependent on the gain (due to the fixed gain bandwidth product of the operational amplifier), the bandwidth of these amplifiers are large. This is due to the fact that in these structures current buffers are operating in open loop without the gain bandwidth product limitation. However as most modern high performance analog integrated circuits incorporate fully differential signal paths [3], a fully differential current buffer can be more beneficial in this case.

The most popular types of current buffers are common gate (CG) stages in CMOS technology, common base (CB) ones in BJT technology [9] and various types of current mirrors which are employed in current mode circuits. Because of single-input single–output structure of these current buffers, fully differential operation is usually provided using multiple current buffers to subtract input signals as is shown in Fig.2 [10]. Unfavorably in this approach tight matching between current buffers is needed to provide a high CMRR. On the other hand increased power consumption and chip area are its other drawbacks.

In this paper a novel low voltage low power fully differential current buffer is introduced. It has a high CMRR and very simple structure. The buffer achieves low input impedance in the case of differential mode inputs and high input impedance for unwanted common mode signals and disturbances. This unique feature further helps to improve its CMRR. The application of the proposed current buffer to realize a voltage amplifier is investigated which shows a voltage amplifier having a -3 dB frequency independent of voltage gain and a high CMRR. Favorably the proposed fully differential current buffer can also be implemented in BIPOLAR technology.

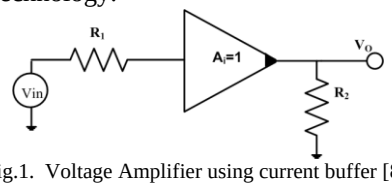

Fig.1. Voltage Amplifier using current buffer [8]

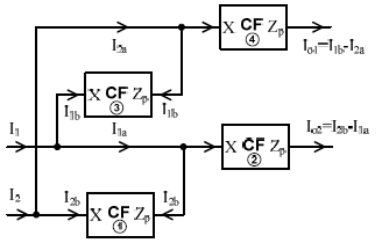

Fig. 2 Fully differential current buffer topology using single input-single output current buffers [10]

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The paper organization is as follows:

Section II presents the proposed fully differential current buffer. Section III describes application of the proposed fully differential current buffer as a high CMRR voltage amplifier with -3dB frequency independent of voltage gain. In Section IV, simulation results are presented and finally section V concludes the paper.

II. Proposed Fully Differential Current Buffer

Fig. 3 shows two CG stages consists of input transistors of M_{N1}-M_{N2} and required bias current sources. The circuit enclosed in dashed rectangle provides bias voltages for the gates of M_{N1}-M_{N2}. The input resistance is 1/gm in which gm is the transconductance of input transistors (M_{N1}-M_{N2}). Unfavorably input resistance is not low enough for most current mode processing circuits. One usual method to reduce the input resistance is increasing transistors gm which results in increasing power consumption. On the other hand structure of Fig.3 has a CMRR of 0 dB. This is mainly due to the fact that, in this structure common mode currents are transferred to the loads along with differential mode ones because there is no mechanism to cancel the common mode inputs.

Structure of Fig.3 can be converted to a fully differential current buffer with high CMRR and low differential mode input impedance as is shown in Fig.4. It is constructed around the circuit of Fig.3 by adding the source coupled pair of M_{S1}-M_{S2}, the PMOS transistors of M_{p1}-M_{p2} and current mirrors M_{B1}-M_{BR1} and M_{B2}-M_{BR2} (instead of bias circuit of I_{bais}-M_{bias} in Fig.3). These extra components are shown in Fig.4 in dashed rectangle. Current mirrors M_{B2}-M_{BR2} along with M_{B1}-M_{BR1} provide high CMRR and M_{S1}-M_{S2} source coupled pair along with M_{P1}-M_{P2}, provide a low differential mode input impedance for the proposed current buffer as will be explained later in this section. By choosing a low bias current for added circuit in dashed line in Fig.4, total power consumption can be reduced.

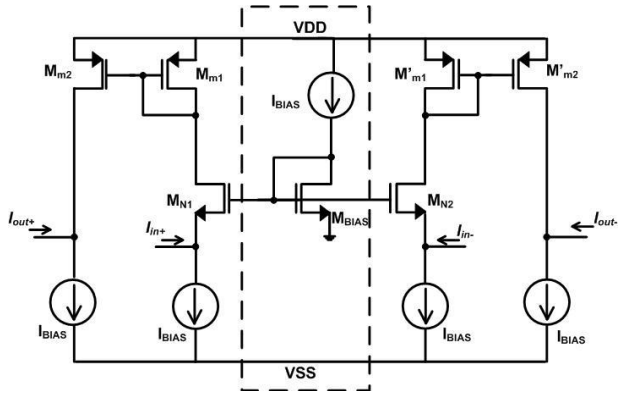


Fig.3. Structure of conventional CG based current buffer

The source coupled pair M_{S1}-M_{S2} plays an important role in the proposed current buffer. In the case of differential mode inputs, the source node of M_{S1}-M_{S2} differential pair (i.e C node) is at virtual ground causing the proposed current buffer to be considered as is shown in Fig.5. As is seen, positive feedback action between M_{N2}-M_{P2} and M_{N1}-M_{P1} forces the input nodes (i.e. in1 and in2 nodes) to be at virtual ground which means a very low differential mode input impedance for the proposed current buffer.

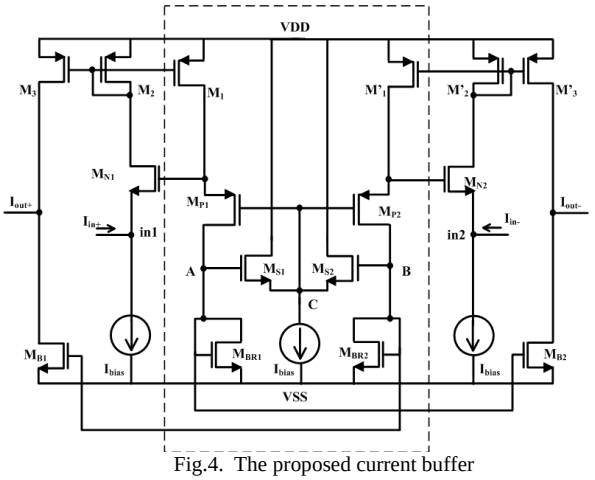


Fig.4. The proposed current buffer

Differential mode input resistance of the proposed current buffer can be found from:

$$R_{ind}=1/gm_n-1/gm_p \quad (1)$$

In which gm_n denotes the input transistors (M_{N1}-M_{N2}) transconductance and gm_p is the tranconduce of M_{P1}-M_{P2}.

The M_{B1}-M_{BR1} and M_{B2}-M_{BR2}current mirrors transfer the differential mode currents to the lower branch of output port (as is shown in Fig.4) where they are added to the upper branch currents transferred to the same port by M2-M3 and M2'-M3' current mirrors. This results in a current gain of two which is beneficial in the case of current amplifiers. To assure the unity value for the current buffer differential mode gain, we have to make aspect ratios of MB1, M3, M'3 and MB2 as one half of the aspect ratios of MBR1,M2,M'2 and MBR2 respectively.

In the case of common mode inputs, voltages at A and B nodes are proportional to the voltages produced at input ports (i.e. in1 and in2). Due to the voltage tracking action of differential pair, voltage at C node is also proportional to the input nodes voltages. So in practice we may assume a simplified circuit for the proposed current buffer in common mode as is shown in Fig.6. In this case no positive feedback action takes place; hence the common mode input resistance won't experience any reduction and can be found from:

$$Rin_c = 1/gm \quad (2)$$

In which gm is the transconductance of input transistors M_{N1}-M_{N2}. Comparing (1) and (2) shows that differential mode input impedance can be made very smaller than the common mode one.

Common mode current of output upper branches are subtracted from each other resulting a very high CMRR

III. Current Buffer Application As A Voltage Amplifier

The proposed current buffer can be used to construct a single input single output voltage amplifier using the configuration of Fig. 1. The voltage gain of this configuration can be found from (31) where R_{in} is the input

impedance of current buffer:

$$A_V = R_2 \big/ (R_1 + R_{in}) \tag{3}$$

As can be found from (3), low input impedance for the current buffer is essential to achieve high voltage gain.
The proposed fully differential current buffer can also be configured as shown in Fig.7 to process differential voltages providing high CMRR and high bandwidth independent of gain. Assuming $R_1=R'_1=R$ and $R_2=R_2'=R_F$, voltage gain and CMRR of this configuration will be:

$$A_V = \frac{V_{O+}}{(Vin_+ - Vin_-)} = -\frac{V_{O-}}{(Vin_+ - Vin_-)} = -\frac{R_F}{(R + R_{ind})} \approx -\frac{R_F}{R} \tag{4}$$

$$CMRR(dB) = CMRR_{cb}(dB) + 20\log 10[\frac{(R + R_{inc})}{(R + R_{ind})}] \tag{5}$$

where $CMRR_{cb}$, R_{inc} and R_{ind} are Current buffers' CMRR, common mode and differential mode input impedances respectively. As can be seen from (5), lower differential mode input impedance of the proposed current buffer compared to common mode one, further helps to increase voltage amplifier CMRR. It is worth noting that, in the conventional current buffer, differential mode input impedance is equal to common mode one (which is equal to 1/gm), as a result, the second term in (5) is zero. While in the proposed current buffer common mode input impedance is much larger than the differential mode one resulting a much higher CMRR.

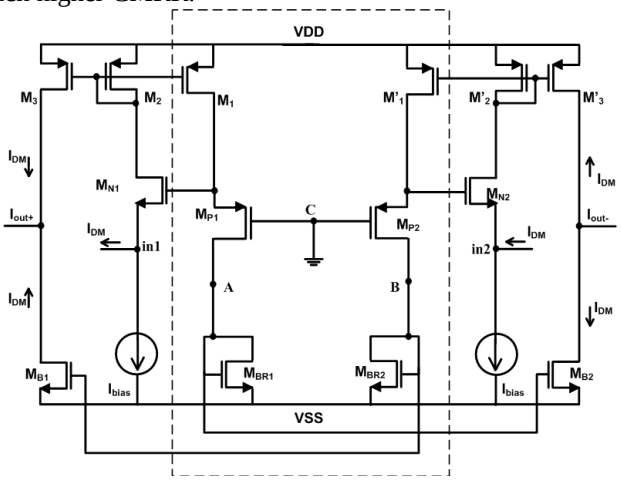


Fig. 5. The proposed current buffer in differential mode.

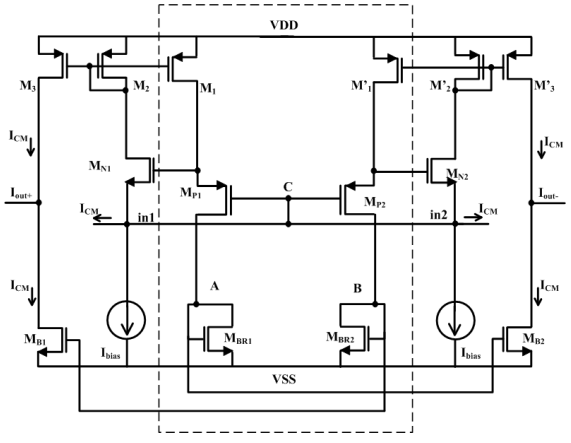


Fig. 6. The proposed current buffer in common mode.

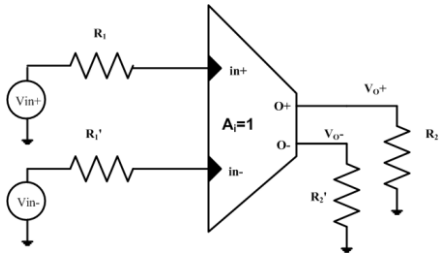


Fig. 7. Voltage Amplifier using proposed current buffer

IV. Simulation Results

The proposed fully differential current buffer is simulated with HSPICE using the model parameters of 0.18µm TSMC CMOS process. The supply voltage is ±0.75V and bias current for all transistors is 20µA except for source coupled pair which is 3.6µA. Transistors aspect ratios are presented in table I and are so chosen to maintain the low input differential impedance, high input common mode impedance and large CMRR of the structure. Current sources are implemented using simple current mirrors with aspect ratio of 10µm/0.5µm.

Fig.8 shows the frequency response of the differential mode and common mode input resistances. As can be seen the proposed current buffer has a differential mode input resistance of 39.5Ω while its common mode input resistance stays at 5.64KΩ which is in the order of 142.7 times larger than differential mode input resistance. The peak value of differential mode input impedance causes no problem because it occurs at frequency around 230MHz which is beyond the bandwidth of the proposed current buffer.

The current gain and -3dB frequency of the proposed current buffer are 0.978 and 77.3MHz respectively shown in fig.9 while its CMRR is 72.2dB which is shown in Fig.10.

To show the correct operation of the proposed current buffer in the case of unbalanced inputs, two sinusoid inputs with amplitudes of I1=5µA and I2=3µA and frequency of 1KHz (Fig.11-a) are applied to it. The produced fully differential outputs are shown in Fig.11-b which prove fully differential operation of the proposed current buffer. Observe that input currents can be written in terms of their common mode (Ic=0.5(I1+I2)) and differential mode (Id=0.5(I1-I2)) components as: I1=Ic+Id and I2=Ic-Id. The differential mode component of input signals (i.e. Id) is successfully appeared at the output ports while the common mode components (i.e. Ic) is eliminated.

Its PSRR+ and PSRR- are 160dB and 122dB respectively. The proposed current buffer has a very high PSRR which makes it very suitable for mixed mode designs.

The time domain analysis of the buffer is done by applying a step input of ±5µA. The result is shown in Fig.12 which proves its sufficient stability.

The power consumption of the proposed buffer is 83.9µW.

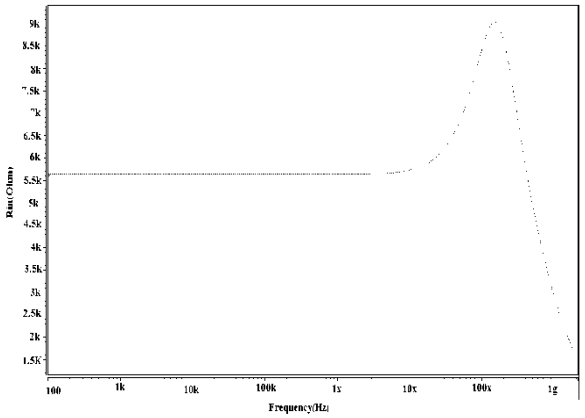
Fig.13 shows a plot of different voltage gains of configuration of Fig.7. The results are achieved with R_1= 1KΩ and R_2 as a parameter. The plot illustrates that the

-3dB bandwidth remains constant at around 20MHz for closed-loop gains from 0dB up to 38.8dB. CMRR of the voltage amplifier in unity gain is 85dB which is 12.2dB

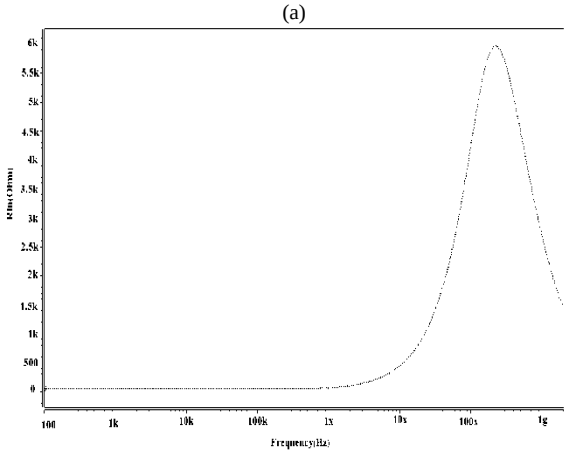
higher than that of the proposed current buffer which is in good agreement with (5).

TABLE I. TRANSISTORS ASPECT RATIOS

Transistor	W/L(μm/μm)
MN1-MN2	10.2/1
MP1-MP2	30/0.5
M1-M2	5/0.5
M'1-M'2	5/0.5
M3-M'3	2.5/0.5
MBR1-MBR2	2/0.5
MB1-MB2	1.21/0.6
MS1-MS2	20/2



(a)



b)

Fig. 8. proposed buffers input resistance frequency performance in Common mode b) Differential mode

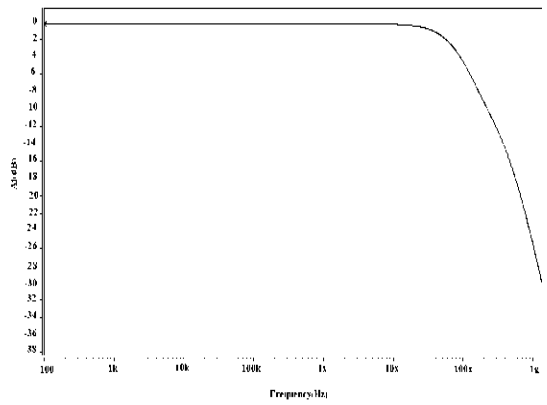


Fig. 9. The proposed current buffer current gain frequency performance

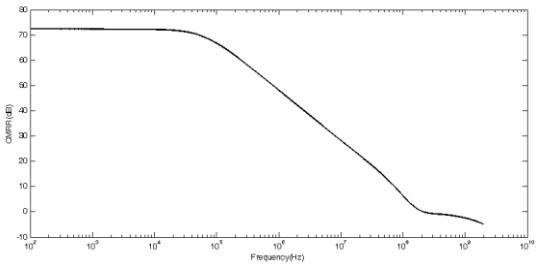
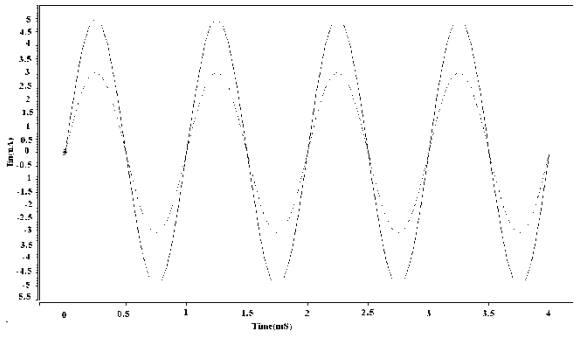
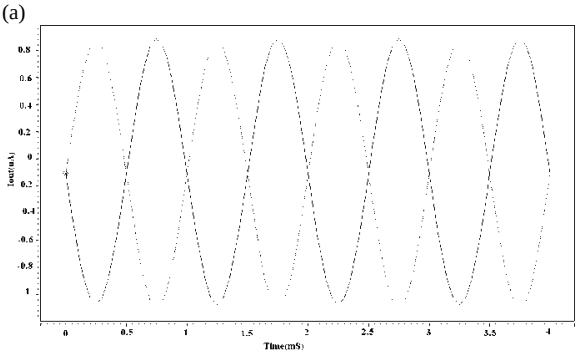


Fig. 10. CMRR frequency performance of the proposed current buffer



(a)



(b)

Fig. 11. Two unbalanced sine inputs(a) produced fully differential outputs(b)

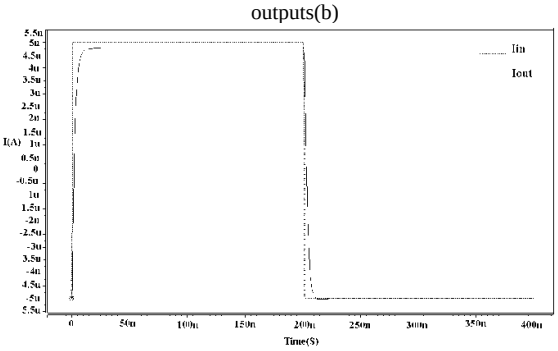


Fig. 12. The proposed current buffer step response

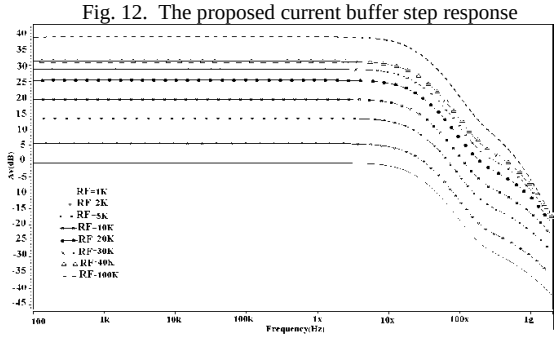


Fig. 13. Voltage amplifier frequency response using the proposed current buffer

V. Conclusion

This paper proposes a novel low voltage low power fully differential current buffer. The proposed current buffer has a unique property of low differential mode input resistance and high common mode one. It has high CMRR and PSRR too. Differential mode low input impedance of the proposed current buffer along with its high CMRR and PSRR makes it suitable for accurate applications. The proposed current buffer is configured as a voltage amplifier demonstrating that contrary to usual voltage amplifiers, its voltage gain is independent from the related -3dB bandwidth.

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